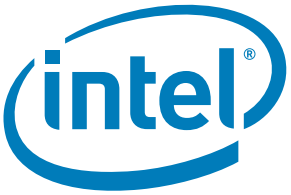
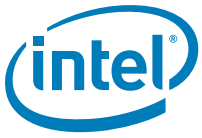


PCIe* 4.0 Retimer Supplemental Features and Standard

BGA Footprint

November 2017

Document Number: 336467-001US



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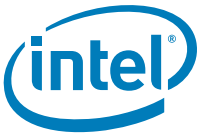
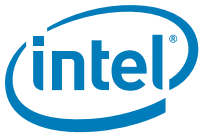


Figures

Tables



Revision History

Document Number	Revision Number	Description	Date
336467	001	• Initial Release	November 2017

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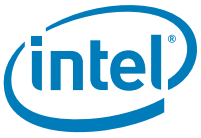


1 Introduction

1.1 Overview

PCI Express* Gen4 capable retimers extend the channel reach on a platform to beyond what is possible otherwise.

With PCI Express Gen4 (16 GT/s), data rate has increased by 2x compared to previous generation (8 GT/s), resulting in shorter channel reach. Common use cases include channels expanding over system boards, backplanes, cables, risers, and add-in cards. Such long channels can have loss that far exceeds the spec loss target of -28 dB at 8 GHz. Retimer is now part of PCI Express 4.0 base specification. PCI-SIG is expected to implement compliance program for testing retimers.

It is expected that significant number of platforms using PCI Express Gen4 will require retimers. Multiple sources of retimers will make adoption of PCIe 4.0 technology easier. Common footprint simplifies the platform design process. Pinout is optimized for 16 GT/s signal integrity and thermal challenges.

Figure 1-1 to Figure 1-4 show few example configurations involving Riser, Mother Board and Add-in Card. Various other configurations are possible.

Figure 1-1. Platform Configuration with an Add-in Card and Retimer on Mother Board

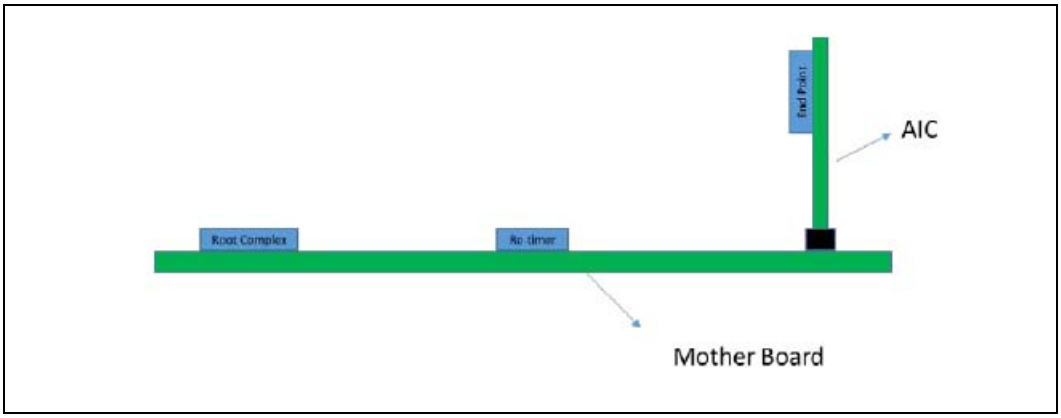


Figure 1-2. Platform Configuration with an Add-in Card and Riser, Retimer on Riser

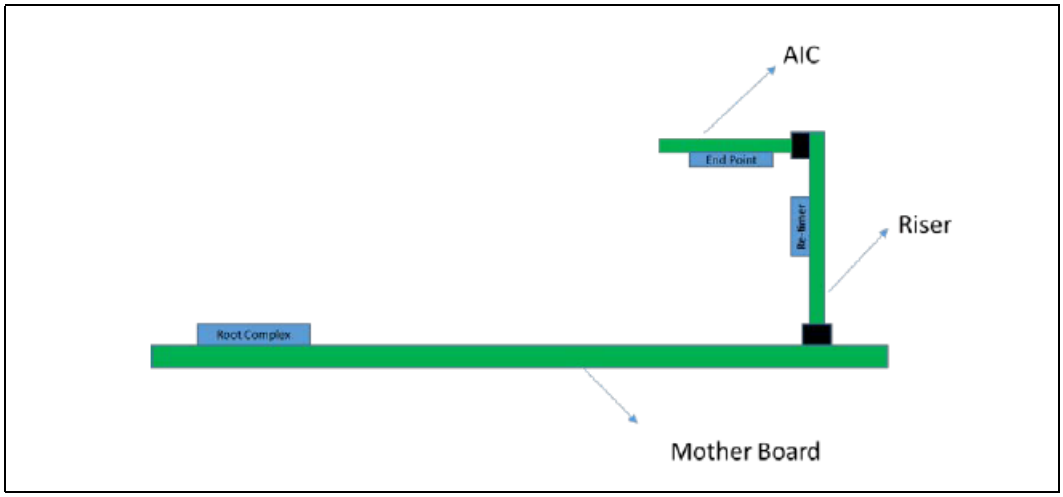


Figure 1-3. Platform Configuration with a Riser and Cable, Retimer is on Riser

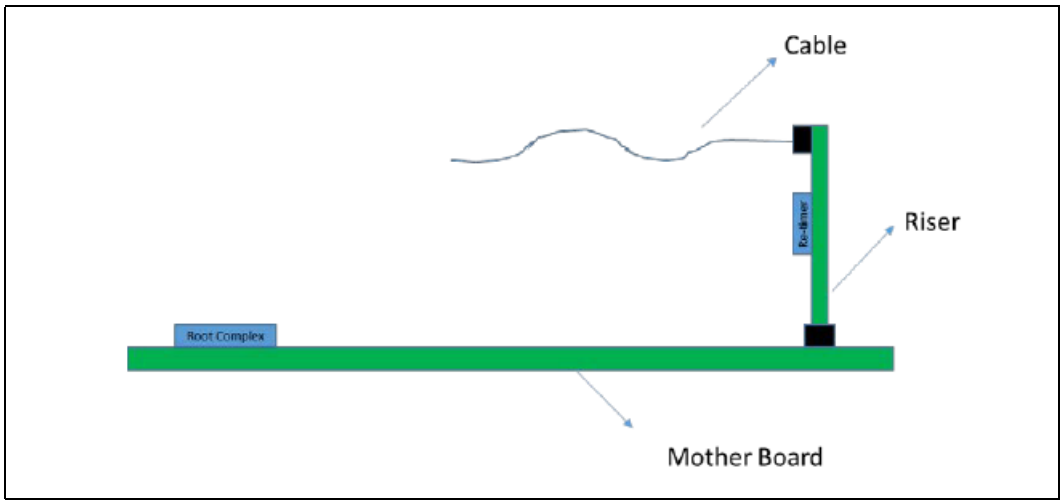
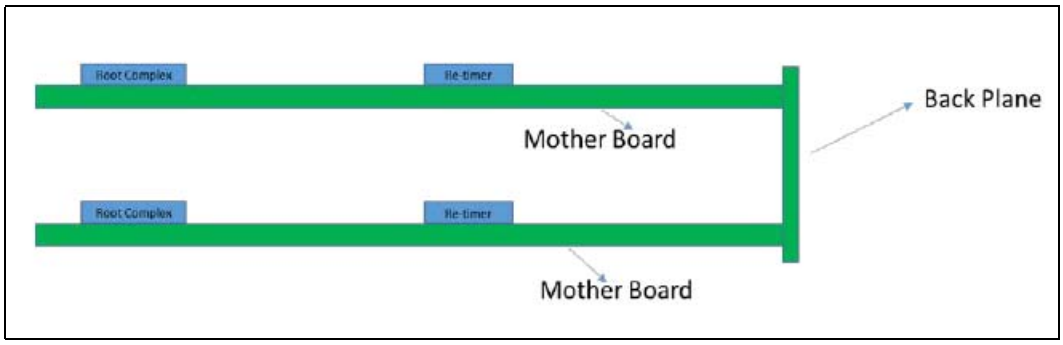
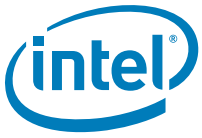


Figure 1-4. Platform Configuration with a Backplane, Retimer on both Mother Boards





1.2 Terminology

The "#" symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when the signal is at a high voltage level.

The following notations are used to describe the various signal types:

Table 1-1. Abbreviations

Term	Description
I	Input
O	Output
I/O	Bi-Directional
PU	Pull-up
PWR	Power
GND	Ground
Host	This term is synonymous with platform or system
NC	No Connect
VD	Vendor Defined
SSC	Spread Spectrum Clocking
SRIS	Separate Reference Clock Independent SSC
RX	PCIe Receiver
TX	PCIe Transmitter
N/A	Not Applicable

1.3 Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- PCI Express Card Electromechanical (CEM) Specification, Revision 4.0, Version 0.5, December 18, 2015
- PCI Express Base Specification, Revision 4.0, Version 0.7, November 11, 2016
- System Management Bus (SMBus) Specification, Version 2.0, August 3, 2000
- JTAG Specification (IEEE 1149.1)
- I2C* BUS Specifications, Version 2.1, January 2000

1.4 Retimer Supplemental Features Beyond PCIe* 4.0 Specification

Table 1-2. Retimer Feature Comparison (Sheet 1 of 2)

Feature	PCIe 4.0 Base Specification for Retimers	PCIe 4.0 for Retimers Supplemental Features and Standard BGA Footprint Specification
SRIS	Optional	Required
Slave Loopback	Optional	Required
Receiver Lane Margining (Voltage)	Optional	Required

Table 1-2. Retimer Feature Comparison (Sheet 2 of 2)

Feature	PCIe 4.0 Base Specification for Retimers	PCIe 4.0 for Retimers Supplemental Features and Standard BGA Footprint Specification
Dynamic Link Subdivision(1) (Bifurcation)	Not defined explicitly but can be supported	Required
L1PM Substates(2)	Optional	Required
SMBus Programmable Configurations	N/A	Required
Support for EEPROM load configuration	N/A	Required
Retimer Common (size, pinout) Footprint	N/A	Required
Reference Clock Out	N/A	Optional

Notes:
1. Dynamic link subdivision should be implemented such that no power reset is required.
2. L1PM Substate support for retimers as defined in Section 4.3.10 in PCIe Base Specification.

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2 Mechanical Specification

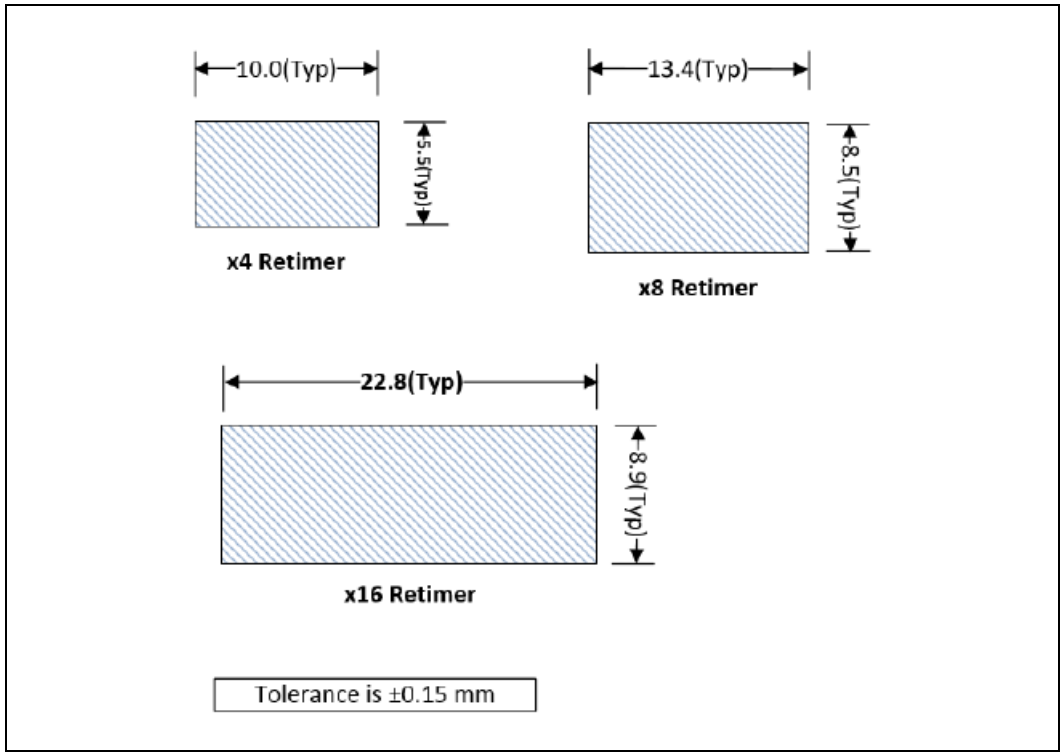
2.1 Overview

Three different retimer package sizes are specified.

- x4: Supports 4 lanes in upstream direction and 4 lanes in downstream direction
- x8: Supports 8 lanes in upstream direction and 8 lanes in downstream direction
- x16: Supports 16 lanes in upstream direction and 16 lanes in downstream direction

The following figure shows the overall package dimensions for the three retimer form factors. Note that all the dimensions are in mm and the tolerance is ±0.15 mm.

Figure 2-1. Retimer Form Factors



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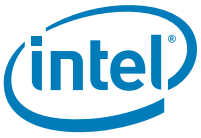


3 Signal Description

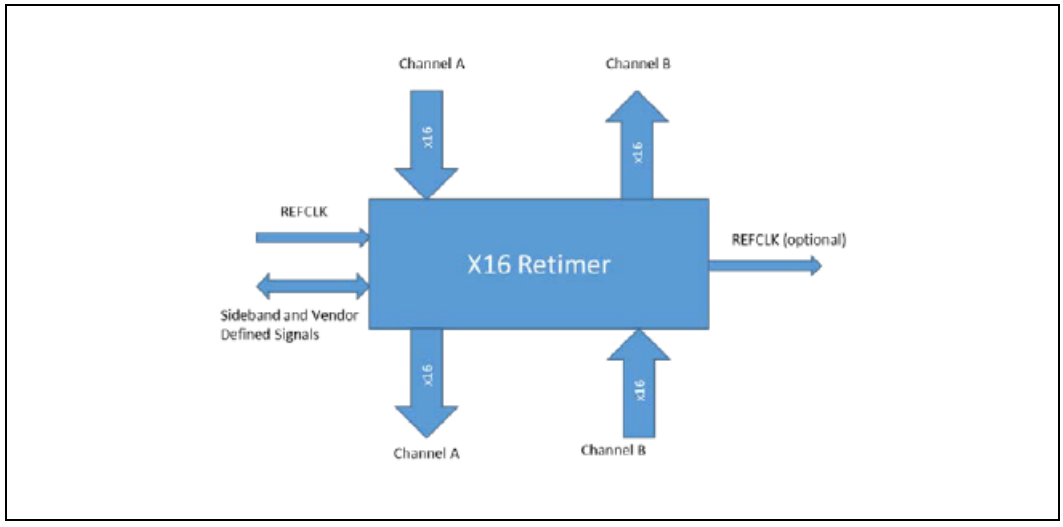
This chapter provides a detailed description of retimer signals. The signal descriptions are arranged in functional groups according to their associated interface. Signal directions in Table 3-1, “x16 Retimer Signal Descriptions”, Table 3-2, “x8 Retimer Signal Descriptions” and Table 3-3, “x4 Retimer Signal Descriptions” are from retimer perspective. that is, “O” indicates output from the retimer device and “I” indicates input to the retimer device**.** Signals labeled “VD” are Vendor Defined and it is assumed that VD balls carry signals that are not critical to retimer basic functionality and are used for providing enhanced or debug features.

Common footprint for following link widths are defined for the PCIe 16 GT/s retimers:

1. x16 (Link with 16 physical lanes)
2. x8 (Link with 8 physical lanes)
3. x4 (Link with 4 physical lanes)

The following figure shows the x16 retimer block diagram. Channel A and Channel B are ports that can be configured to be upstream or downstream.

Figure 3-1. x16 Retimer Block Diagram



3.1 x16 Retimer Interface Signals

The following table lists pin numbers and functions for each of the pins in the x16 pinout, along with voltage level wherever applicable.

Table 3-1. x16 Retimer Signal Descriptions (Sheet 1 of 6)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/O				
M26	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
P29	A_PETn0	O		

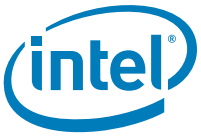


Table 3-1. x16 Retimer Signal Descriptions (Sheet 2 of 6)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
W26	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
AA29	A_PETn1	O		
AF26	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
AH29	A_PETn2	O		
AN26	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
AR29	A_PETn3	O		
AY26	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
BB29	A_PETn4	O		
BG26	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
BJ29	A_PETn5	O		
BP26	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
BT29	A_PETn6	O		
CA26	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
CC29	A_PETn7	O		
CH26	A_PETp8	O	Transmitter differential pair, A Channels, Lane 8	
CK29	A_PETn8	O		
CR26	A_PETp9	O	Transmitter differential pair, A Channels, Lane 9	
CU29	A_PETn9	O		
DB26	A_PETp10	O	Transmitter differential pair, A Channels, Lane 10	
DD29	A_PETn10	O		
DJ26	A_PETp11	O	Transmitter differential pair, A Channels, Lane 11	
DL29	A_PETn11	O		
DT26	A_PETp12	O	Transmitter differential pair, A Channels, Lane 12	
DV29	A_PETn12	O		
EC26	A_PETp13	O	Transmitter differential pair, A Channels, Lane 13	
EE29	A_PETn13	O		
EK26	A_PETp14	O	Transmitter differential pair, A Channels, Lane 14	
EM29	A_PETn14	O		
EU26	A_PETp15	O	Transmitter differential pair, A Channels, Lane 15	
EW29	A_PETn15	O		
N34	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
R35	B_PERn0	I		
Y34	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
AB35	B_PERn1	I		
AG34	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
AJ35	B_PERn2	I		
AP34	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
AT35	B_PERn3	I		
BA34	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
BC35	B_PERn4	I		

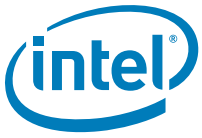


Table 3-1. x16 Retimer Signal Descriptions (Sheet 3 of 6)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
BH34	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
BK35	B_PERn5	I		
BR34	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
BU35	B_PERn6	I		
CB34	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
CD35	B_PERn7	I		
CJ34	B_PERp8	I	Receiver differential pair, B Channels, Lane 8	
CL35	B_PERn8	I		
CT34	B_PERp9	I	Receiver differential pair, B Channels, Lane 9	
CV35	B_PERn9	I		
DC34	B_PERp10	I	Receiver differential pair, B Channels, Lane 10	
DE35	B_PERn10	I		
DK34	B_PERp11	I	Receiver differential pair, B Channels, Lane 11	
DM35	B_PERn11	I		
DU34	B_PERp12	I	Receiver differential pair, B Channels, Lane 12	
DW35	B_PERn12	I		
ED34	B_PERp13	I	Receiver differential pair, B Channels, Lane 13	
EF35	B_PERn13	I		
EL34	B_PERp14	I	Receiver differential pair, B Channels, Lane 14	
EN35	B_PERn14	I		
EV34	B_PERp15	I	Receiver differential pair, B Channels, Lane 15	
EY35	B_PERn15	I		
R1	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
N2	A_PERn0	I		
AB1	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
Y2	A_PERn1	I		
AJ1	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
AG2	A_PERn2	I		
AT1	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
AP2	A_PERn3	I		
BC1	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
BA2	A_PERn4	I		
BK1	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
BH2	A_PERn5	I		
BU1	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
BR2	A_PERn6	I		
CD1	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
CB2	A_PERn7	I		
CL1	A_PERp8	I	Receiver differential pair, A Channels, Lane 8	
CJ2	A_PERn8	I		

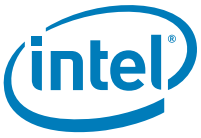


Table 3-1. x16 Retimer Signal Descriptions (Sheet 4 of 6)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
CV1	A_PERp9	I	Receiver differential pair, A Channels, Lane 9	
CT2	A_PERn9	I		
DE1	A_PERp10	I	Receiver differential pair, A Channels, Lane 10	
DC2	A_PERn10	I		
DM1	A_PERp11	I	Receiver differential pair, A Channels, Lane 11	
DK2	A_PERn11	I		
DW1	A_PERp12	I	Receiver differential pair, A Channels, Lane 12	
DU12	A_PERn12	I		
EF1	A_PERp13	I	Receiver differential pair, A Channels, Lane 13	
ED2	A_PERn13	I		
EN1	A_PERp14	I	Receiver differential pair, A Channels, Lane 14	
EL2	A_PERn14	I		
EY1	A_PERp15	I	Receiver differential pair, A Channels, Lane 15	
EV2	A_PERn15	I		
M7	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
P10	B_PETn0	O		
W7	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
AA10	B_PETn1	O		
AF7	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
AH10	B_PETn2	O		
AN7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
AR10	B_PETn3	O		
AY7	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
BB10	B_PETn4	O		
BG7	B_PETp5	O	Transmitter differential pair, B Channels, Lane 5	
BJ10	B_PETn5	O		
BP7	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
BT10	B_PETn6	O		
CA7	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
CC10	B_PETn7	O		
CH7	B_PETp8	O	Transmitter differential pair, B Channels, Lane 8	
CK10	B_PETn8	O		
CR7	B_PETp9	O	Transmitter differential pair, B Channels, Lane 9	
CU10	B_PETn9	O		
DB7	B_PETp10	O	Transmitter differential pair, B Channels, Lane 10	
DD10	B_PETn10	O		
DJ7	B_PETp11	O	Transmitter differential pair, B Channels, Lane 11	
DL10	B_PETn11	O		
DT7	B_PETp12	O	Transmitter differential pair, B Channels, Lane 12	
DV10	B_PETn12	O		

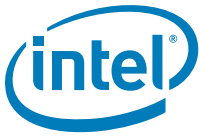


Table 3-1. x16 Retimer Signal Descriptions (Sheet 5 of 6)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
EC7	B_PETp13	O	Transmitter differential pair, B Channels, Lane 13	
EE10	B_PETn13	O		
EK7	B_PETp14	O	Transmitter differential pair, B Channels, Lane 14	
EM10	B_PETn14	O		
EU7	B_PETp15	O	Transmitter differential pair, B Channels, Lane 15	
EW10	B_PETn15	O		
Reference Clock				
FJ16	REFCLK+	I	100MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the PCIe Base Specification	
FF18	REFCLK-	I		
PCI Express Auxiliary Signals				
F2	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
G35	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
B6	JTAG_TDI	I	JTAG Test Data In	1.8 V(3.3 V tolerant)
B9	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the IO voltage selected for other JTAG signals	
B12	JTAG_TMS	I	JTAG Test Mode Select	1.8 V(3.3 V tolerant)
B3	JTAG_TCK	I	JTAG Clock	1.8 V(3.3 V tolerant)
E8	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V(3.3 V tolerant)
System Management Bus (SMBus)				
B31	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V(3.3 V tolerant)
B28	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V(3.3 V tolerant)
F34	SMB_ADDR_0	I	SMBus Address Bit0	1.8 V(3.3 V tolerant)
B23	SMB_ADDR_1	I	SMBus Address Bit1	1.8 V(3.3 V tolerant)
B25	SMB_ADDR_2/ VD_18(1)	I	SMBus Address Bit2 or Vendor Defined	1.8 V(3.3 V tolerant)

Table 3-1. x16 Retimer Signal Descriptions (Sheet 6 of 6)

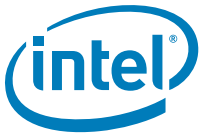
Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
EEPROM Configuration Interface				
FJ3	EE_DAT/VD_7(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8 V(3.3 V tolerant)
FF5	EE_CLK/VD_8(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8 V(3.3 V tolerant)
Miscellaneous				
FJ23	VD_1(1)	TBD	Vendor Defined Signal	
FF24	VD_2(1)	TBD	Vendor Defined Signal	
FJ6	VD_3(1)	TBD	Vendor Defined Signal	
FF8	VD_4(1)	TBD	Vendor Defined Signal	
FJ9	VD_5(1)	TBD	Vendor Defined Signal	
FF11	VD_6(1)	TBD	Vendor Defined Signal	
FJ25	VD_9(1)	TBD	Vendor Defined Signal	
FF27	VD_10(1)	TBD	Vendor Defined Signal	
FJ28	VD_11(1)	TBD	Vendor Defined Signal	
FF30	VD_12(1)	TBD	Vendor Defined Signal	
FJ31	VD_13(1)	TBD	Vendor Defined Signal	
FF33	VD_14(1)	TBD	Vendor Defined Signal	
G1	VD_15(1)	TBD	Vendor Defined Signal	
B16	REFCLK_Out+ (2)	O	100MHz. This pin is used for driving REFCLK_out+	
E18	REFCLK_Out1 (2)	O	100MHz. This pin is used for driving REFCLK_out -	
E11	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
6 pins	PWR_1	Power Rail 1	1.8V or 3.3V	
24 pins	PWR_2	Power Rail 2	1.1V or 1.0V or 0.9V or 0.8V	
152pins	GND		0V	

Notes:
1. It is safe to route high speed Vendor Defined (VD) signals at these locations. Care must be taken to provide enough GND isolation. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out, when supported, is compliant with REFCLK definition in the PCIe Base Specification.

3.1.1 Signal Descriptions

3.1.1.1 SMBus Interface

SMBCLK, SMBDAT and three address pins (SMB_ADDR_0, SMB_ADDR_1, SMB_ADDR_2) are assigned in the ballmap. Three address bits are required to address retimers on the SMBus in a platform configuration. Retimer vendors are allowed to take care of SMBus address needs on the platform by using only two address pins, if they can take care of additional addresses needed by the platform in a proprietary way. The retimer vendors can use the third address bit for Vendor Defined purposes in that case. Address pin SMB_ADDR_2 can be used for Vendor Defined signal..



3.1.1.2 EEPROM Interface

EECLK and EEDAT signals are defined to load initial configuration from an external EEPROM. No specific interface is mentioned, giving retimer vendors freedom to use the interface of their choice. An example of the interface that can be used is I2C.

When this dedicated interface is not used for EEPROM load, and some other means are used to load EEPROM configuration, these pin can be used as Vendor Defined.

3.1.1.3 Miscellaneous Signals

3.1.1.3.1 RX_DET_BYP (PCIe_BYPASS_MODE)

This signal is asserted to bypass the Receiver detection process to expedite the link training. In this mode, the retimer does not do any active determination of its Receiver impedance. It rather assumes that the receiver is present on the other end of the link. This feature can be used for soldered-down devices. The same signal when asserted, also serves to bypass the PCIe mode.

3.1.1.3.2 REFCLK_Out+ / REFCLK_Out-

This is the 100 MHz reference clock as defined by the PCIe Base Specification. Some retimer devices may provide this clock output to ease clock routing complexities on the platform. Retimer devices that do not support REFCLK_Out feature are allowed to use these pins for Vendor Defined purposes.

3.1.1.3.3 PERST#

Fundamental Reset signal as defined by the PCIe Base Specification.

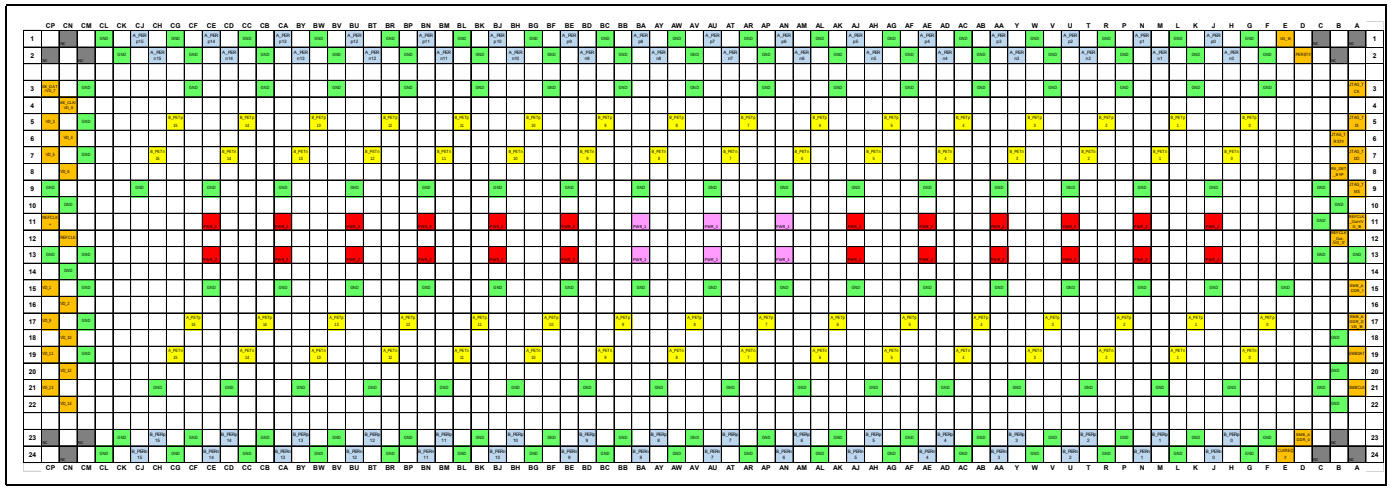
3.1.1.3.4 CLKREQ#

This signal is used to support L1PM Substates. Refer to the PCIe Base Specification for more details on L1PM Substate support for retimers.

3.2 x16 Retimer Ballmap (Package Side)

The following figure shows the ball arrangement from the retimer package side. Note that this figure is for reference only, for actual pin number and spacing details, refer to Figure 3-5, “x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)” on page 23.

Figure 3-2. x16 Retimer, Package Side Pin Arrangement (Top View)



Note: Refer to Figure 3-5, “x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)” on page 23 for pitch and spacing details.

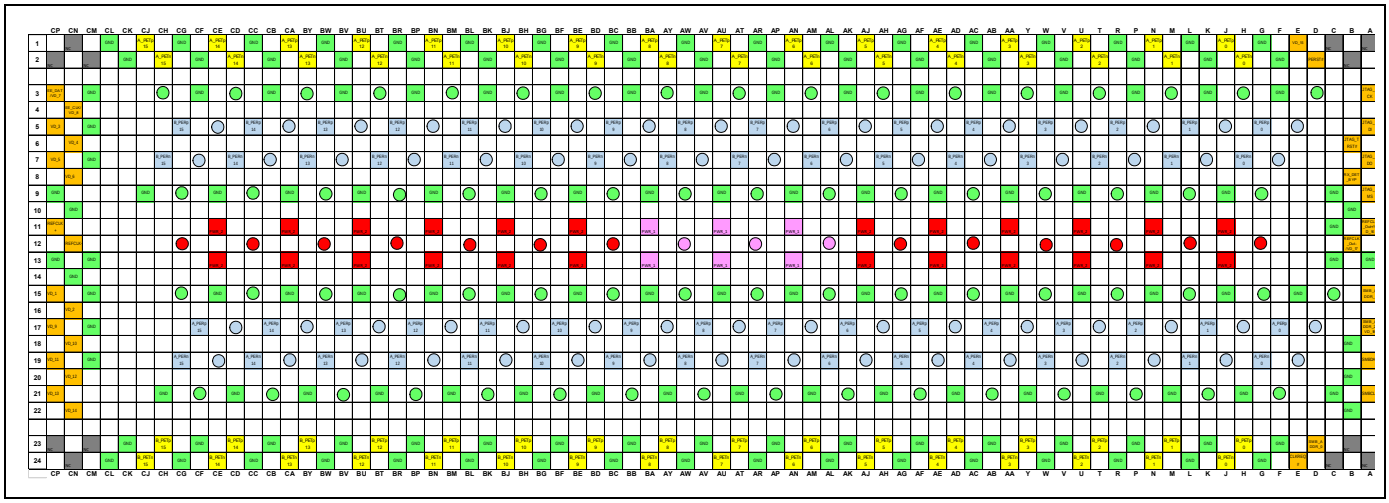
Legend	
	PWR_1
	PWR_2
	GND
	Control and VD Signals
	Differential TX
	Differential RX
	No Balls
	NC

3.3 x16 Retimer, Platform side Pin Arrangement

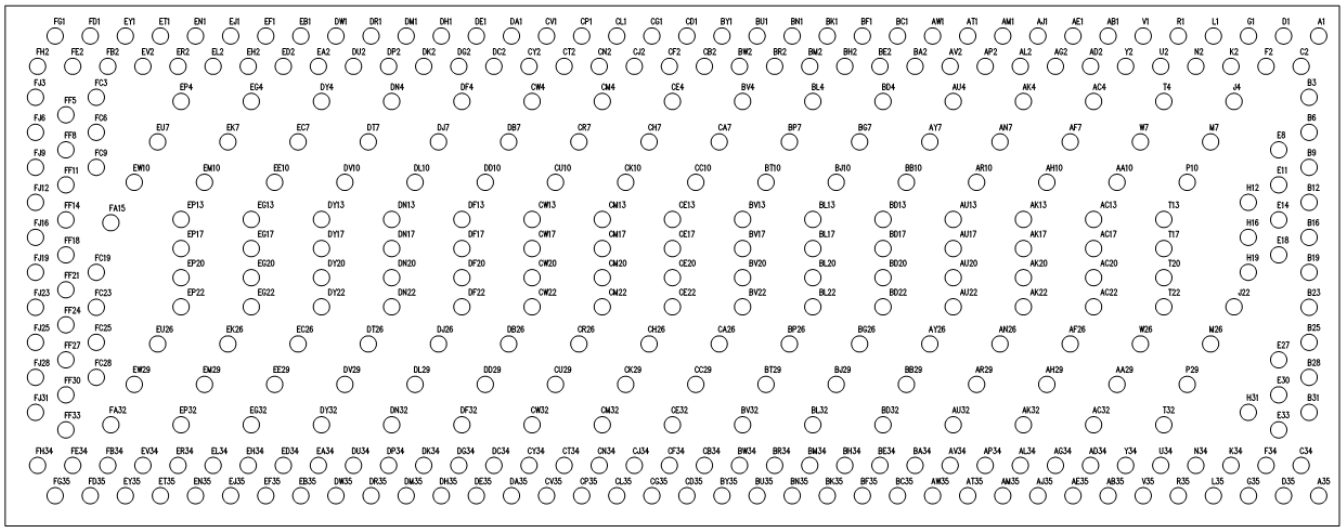
The following figure shows the platform side pin arrangement with PCB vias. The TX and RX balls here have been swapped when compared to package side ballmap (Figure 3-2). That is, “TX lane x” in package side ballmap gets mapped to “RX lane x” in the land pattern.

Note that this figure is for reference only; for actual pin number and spacing details, refer to Figure 3-5, “x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)” on page 23.

Figure 3-3. x16 Retimer, Platform side Pin Arrangement (Top View)



Legend	
	RX Via
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via



3.4 x16 Retimer Package-side Ball Arrangement

The following figure shows the top view of x16 retimer package-side ball arrangement with pin numbers.

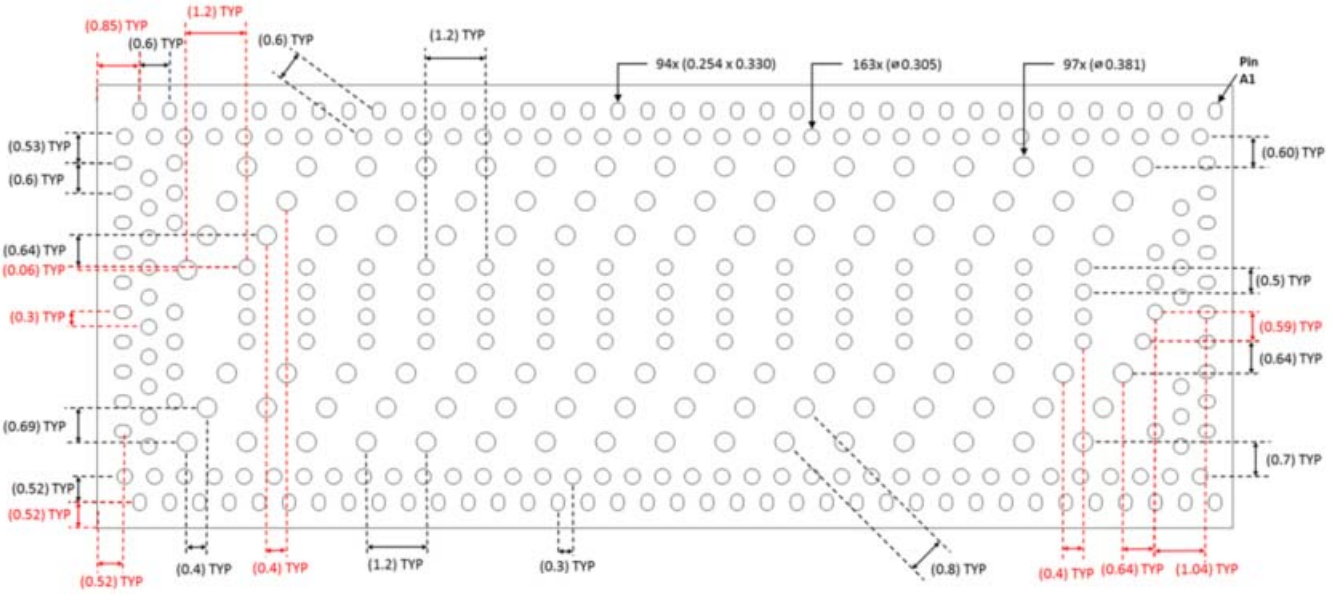
Figure 3-4. x16 Retimer, Physical Ballmap on Package (Top View)

3.5 x16 Retimer Platform-side Land Pattern

The following figure shows top view of the platform side mechanical outline drawing for x16 retimer.

Dimension tolerances for ball diameter are ±0.05 mm.

Figure 3-5. x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.6 x8 Retimer Interface Signals

Table 3-2. x8 Retimer Signal Descriptions (Sheet 1 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
B9	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A10	A_PETn0	O		
C6	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
D7	A_PETn1	O		
B3	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
A4	A_PETn2	O		
E2	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
D1	A_PETn3	O		
AB1	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
AA2	A_PETn4	O		

Table 3-2. x8 Retimer Signal Descriptions (Sheet 2 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
AE4	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
AD3	A_PETn5	O		
AH1	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
AG2	A_PETn6	O		
AL4	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
AK3	A_PETn7	O		
B15	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A14	A_PERn0	I		
C18	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
D17	A_PERn1	I		
B21	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
A20	A_PERn2	I		
E22	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
D23	A_PERn3	I		
AB23	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
AA22	A_PERn4	I		
AE20	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
AD21	A_PERn5	I		
AH23	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
AG22	A_PERn6	I		
AL20	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
AK21	A_PERn7	I		
H21	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
G20	B_PETn0	O		
L22	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
K23	B_PETn1	O		
P21	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
N20	B_PETn2	O		
U22	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
T23	B_PETn3	O		
AP23	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
AN22	B_PETn4	O		
AU20	B_PETp5	O	Transmitter differential pair B Channels, Lane 5	
AT21	B_PETn5	O		
AP17	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
AR18	B_PETn6	O		
AU14	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
AT15	B_PETn7	O		
H3	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
G4	B_PERn0	I		

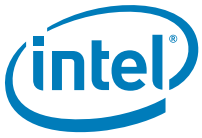


Table 3-2. x8 Retimer Signal Descriptions (Sheet 3 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
L2	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
K1	B_PERn1	I		
P3	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
N4	B_PERn2	I		
U22	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
T1	B_PERn3	I		
AP1	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
AN2	B_PERn4	I		
AU4	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
AT3	B_PERn5	I		
AP7	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
AR6	B_PERn6	I		
AU10	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
AT9	B_PERn7	I		
Reference Clock				
Y5	REFCLK+	I	100 MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the PCIe Base Specification	
V5	REFCLK-	I		
PCI Express Auxiliary Signals				
Y1	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
B11	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
AC18	JTAG_TDI	I	JTAG Test Data In	1.8 V (3.3 V tolerant)
L18	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the IO voltage selected for other JTAG signals	
E16	JTAG_TMS	I	JTAG Test Mode Select	1.8 V (3.3 V tolerant)
AG18	JTAG_TCK	I	JTAG Clock	1.8 V (3.3 V tolerant)
R18	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V (3.3 V tolerant)
System Management Bus (SMBus)				
AC6	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V (3.3 V tolerant)
AG6	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V (3.3 V tolerant)
R6	SMB_ADDR_0	I	SMBus Address Bit 0	1.8 V (3.3 V tolerant)
L6	SMB_ADDR_1	I	SMBus Address Bit 1	1.8 V (3.3 V tolerant)
V23	SMB_ADDR_2/ VD_15	I	SMBus Address Bit2 or Vendor Defined	1.8 V (3.3 V tolerant)
EEPROM Configuration Interface				
AP11	EE_DAT/VD_5(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8 V (3.3 V tolerant)
AP13	EE_CLK/VD_6(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8 V (3.3 V tolerant)
Miscellaneous				
AT1	VD_1	TBD	Vendor Defined Signal	

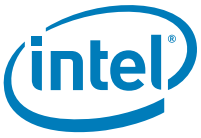


Table 3-2. x8 Retimer Signal Descriptions (Sheet 4 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
W2	VD_2	TBD	Vendor Defined Signal	
B1	VD_3	TBD	Vendor Defined Signal	
AU12	VD_4	TBD	Vendor Defined Signal	
D11	VD_7(1)	TBD	Vendor Defined Signal	
D13	VD_8(1)	TBD	Vendor Defined Signal	
A12	VD_9	TBD	Vendor Defined Signal	
W22	VD_10	TBD	Vendor Defined Signal	
AT23	VD_11	TBD	Vendor Defined Signal	
V23	VD_12	TBD	Vendor Defined Signal	
B23	VD_13	TBD	Vendor Defined Signal	
AT13	REFCLK_Out+ (2)	O	100MHz. This pin is used for driving REFCLK_out+	
Y19	REFCLK_Out1 (2)	O	100MHz. This pin is used for driving REFCLK_out -	
V19	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
16 pins	PWR_1	Power Rail 1	1.8V or 3.3V	
48 pins	PWR_2	Power Rail 2	1.1V or 1.0V or 0.9V or 0.8V	
175pins	GND		0V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static/ quasi static (low slew rate) signals. Routing high frequency signals on these may impose crosstalk on high-speed signals. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out, when supported is compliant with REFCLK definition in the PCIe Base Specification.

3.6.1 Signal Descriptions

3.6.1.1 SMBus Interface

Refer to Section 3.1.1.1, “SMBus Interface” on page 18.

3.6.1.2 EEPROM Interface

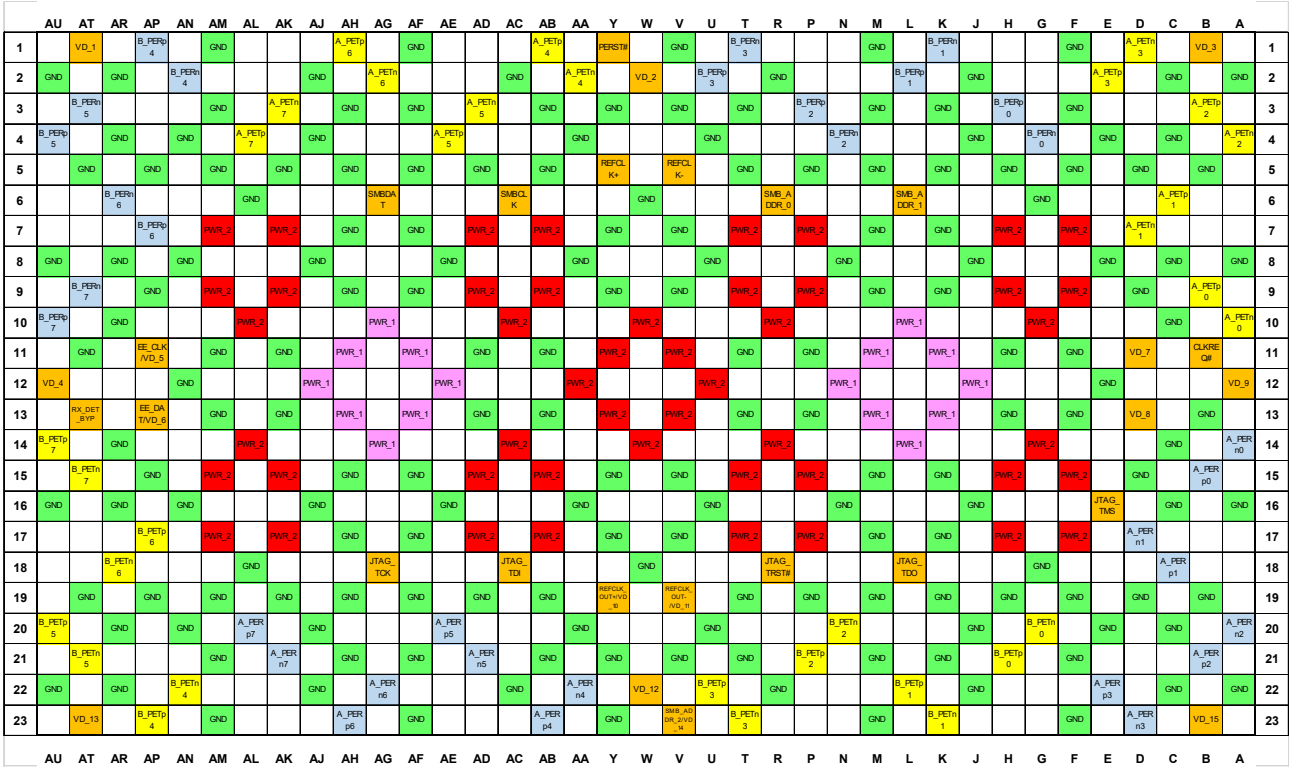
Refer to Section 3.1.1.2, “EEPROM Interface” on page 19

3.6.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, “Miscellaneous Signals” on page 19.

3.7 x8 Retimer Ballmap

Figure 3-6. x8 Retimer, Package-side Pin Arrangement (Top View)

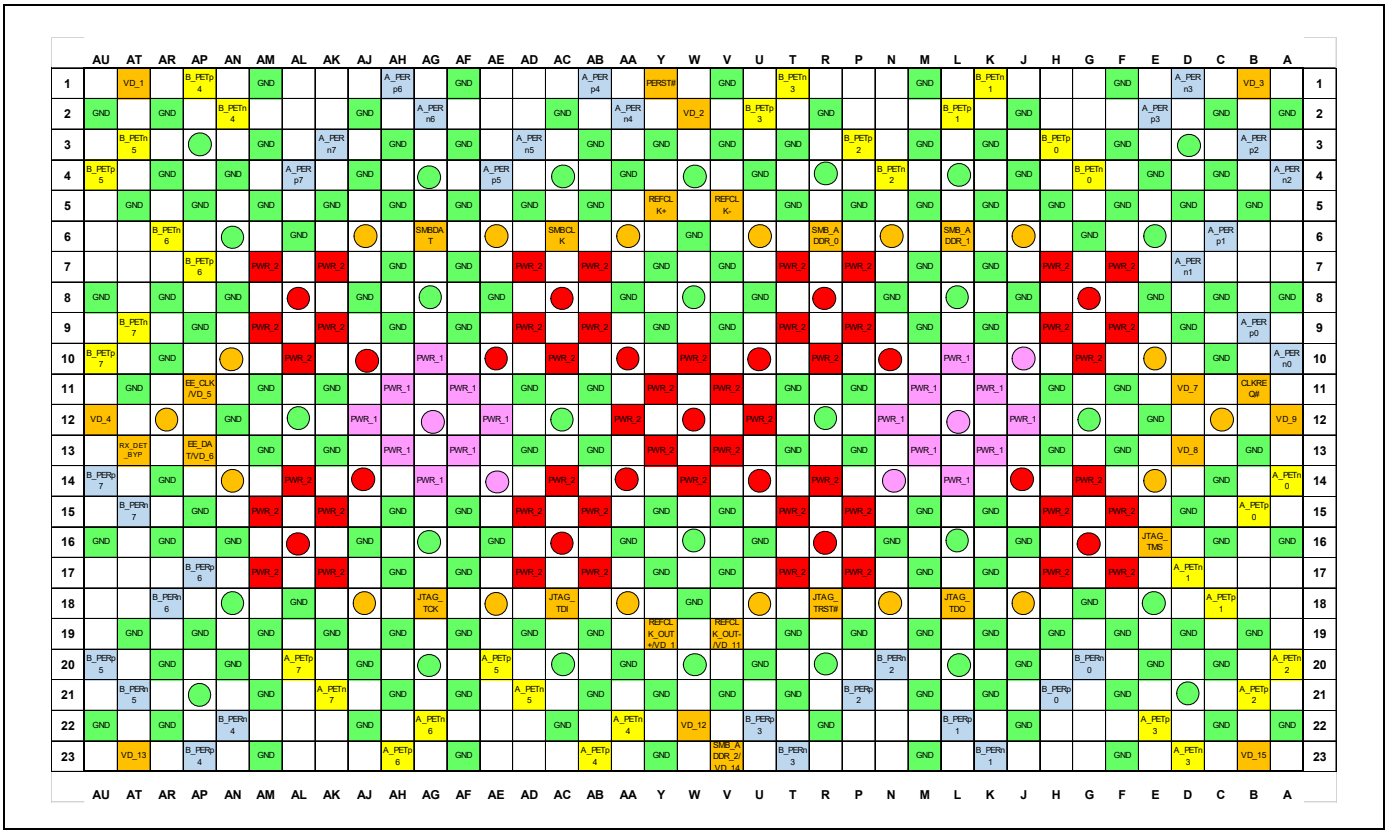


Legend	
	PWR_1
	PWR_2
	GND
	Control Signals
	Differential TX
	Differential RX
	No Balls

3.8 X8 Retimer, Platform-side Land Pattern

The following figure shows the platform side land pattern. The TX and RX balls have been swapped when compared to package side ballmap. i.e. “TX lane x” in package side ballmap gets mapped to “RX lane x” in the land pattern.

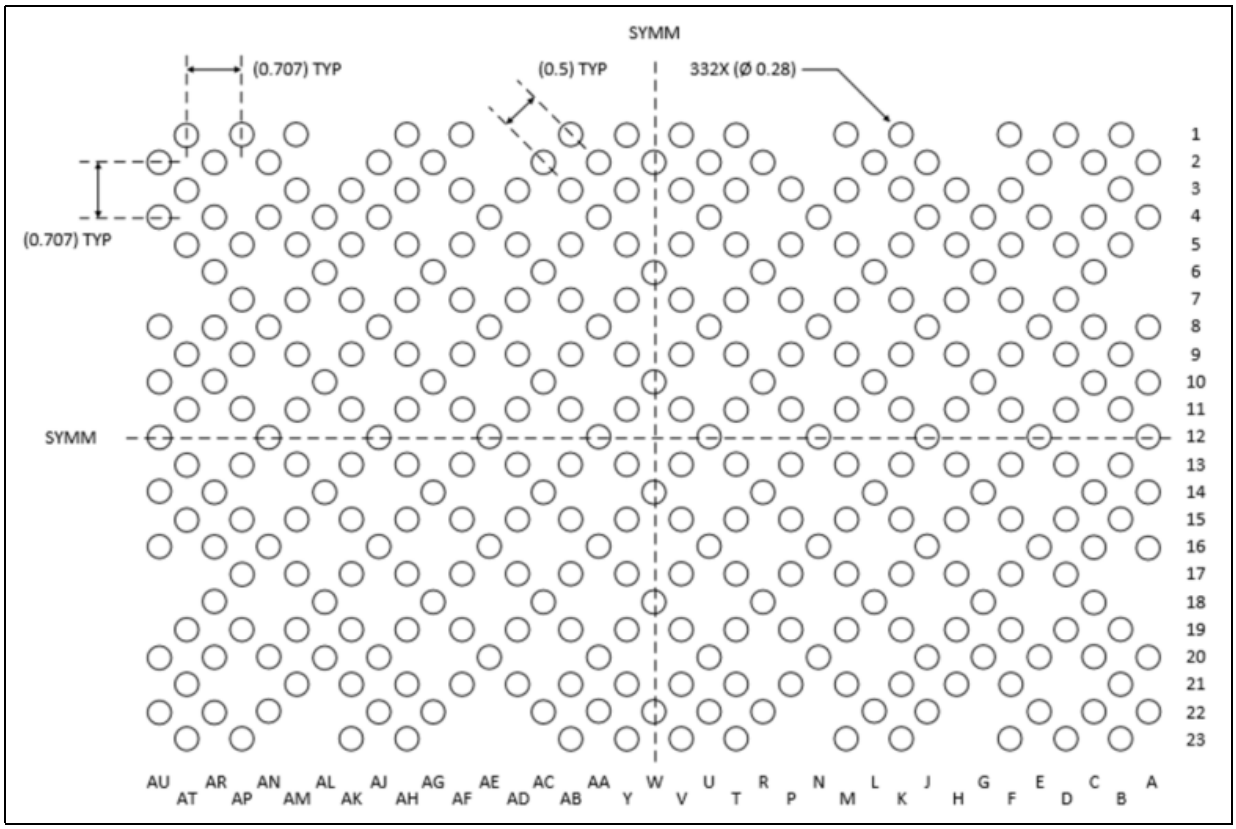
Figure 3-7. x8 Retimer, Platform-side Pin Arrangement (Top View)



Legend	
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via

3.9 x8 Retimer Package-side Ballmap

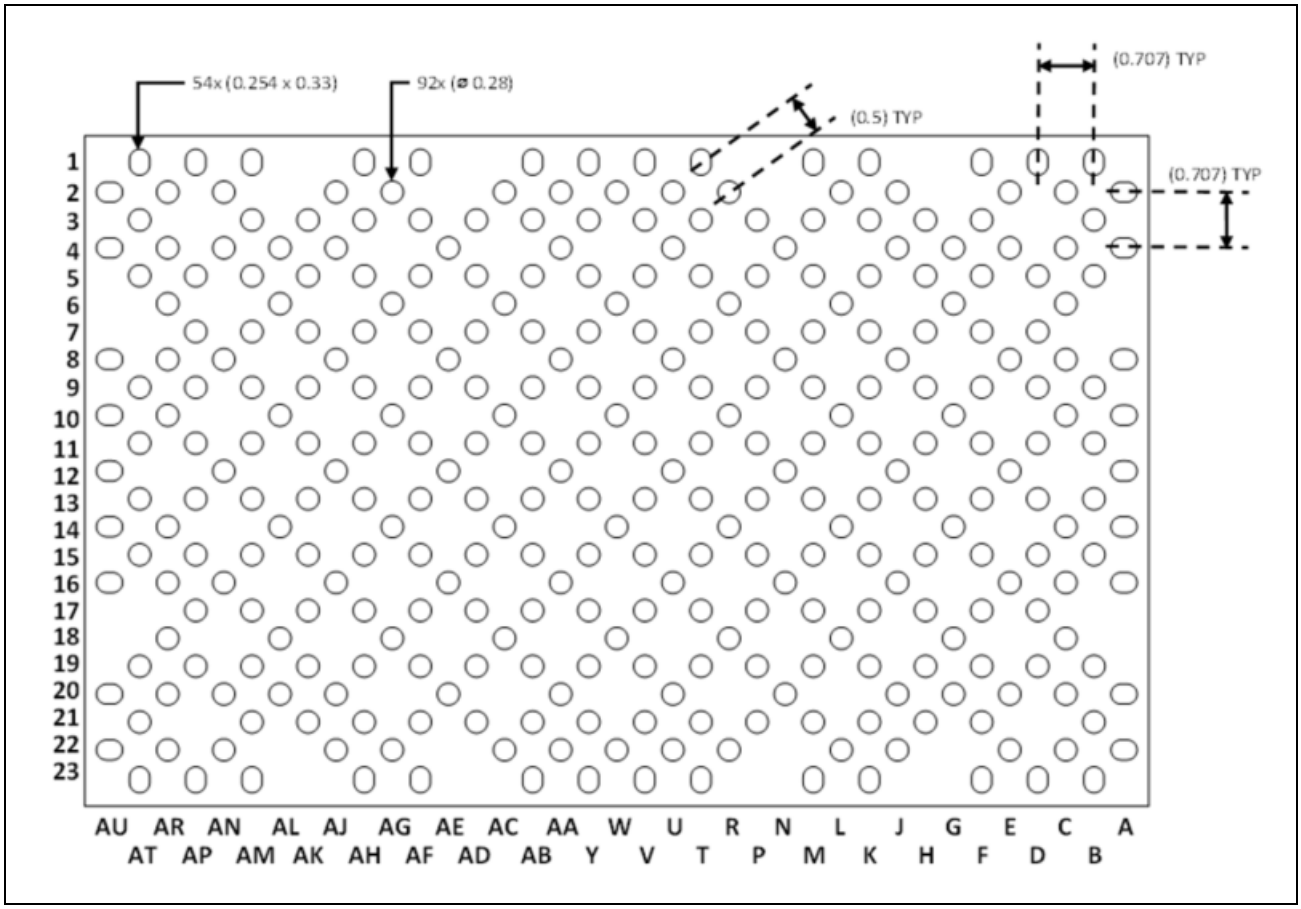
Figure 3-8. x8 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.10 x8 Retimer Platform-side Land Pattern

Figure 3-9. x8 Retimer, Platform-side Land Pattern with Spacing Details (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.11 x4 Retimer Interface Signals

Table 3-3. x4 Retimer Signal Descriptions (Sheet 1 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
A3	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A4	A_PETn0	O		
C1	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
B1	A_PETn1	O		
F1	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
E1	A_PETn2	O		

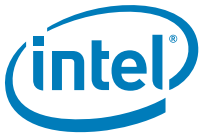


Table 3-3. x4 Retimer Signal Descriptions (Sheet 2 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
J1	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
H1	A_PETn3	O		
A8	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A7	A_PERn0	I		
C10	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
B10	A_PERn1	I		
F10	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
E10	A_PERn2	I		
J10	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
H10	A_PERn3	I		
M10	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
I10	B_PETn0	O		
R10	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
P10	B_PETn1	O		
V10	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
U10	B_PETn2	O		
W7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
W8	B_PETn3	O		
M1	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
L1	B_PERn0	I		
R1	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
P1	B_PERn1	I		
V1	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
U1	B_PERn2	I		
W4	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
W3	B_PERn3	I		
Reference Clock				
C5	REFCLK+	I	100MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the PCIe Base Specification	
C6	REFCLK-	I		
PCI Express Auxiliary Signals				
A2	PERST#	I	Fundamental Reset; Active Low	1.8 V (3.3 V tolerant)
A9	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8 V (3.3 V tolerant)
JTAG				
U3	JTAG_TDI	I	JTAG Test Data In	1.8 V (3.3 V tolerant)
C3	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the IO voltage selected for other JTAG signals	
N3	JTAG_TMS	I	JTAG Test Mode Select	1.8 V (3.3 V tolerant)
K3	JTAG_TCK	I	JTAG Clock	1.8 V (3.3 V tolerant)
J3	JTAG_TRST#	I	JTAG Reset; Active Low	1.8 V (3.3 V tolerant)

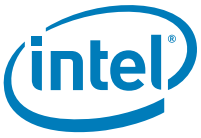


Table 3-3. x4 Retimer Signal Descriptions (Sheet 3 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
System Management Bus (SMBus)				
G8	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8 V (3.3 V tolerant)
K8	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8 V (3.3 V tolerant)
W5	SMB_ADDR_0	I	SMBus Address Bit 0	1.8 V (3.3 V tolerant)
W6	SMB_ADDR_1	I	SMBus Address Bit 1	1.8 V (3.3 V tolerant)
W9	SMB_ADDR_2/ VD_12	I	SMBus Address Bit2 or Vendor Defined	1.8 V (3.3 V tolerant)
EEPROM Configuration Interface				
U8	EE_DAT/VD_9(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8 V(3.3 V tolerant)
N8	EE_CLK/VD_10(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8 V(3.3 V tolerant)
Miscellaneous				
W1	VD_1	TBD	Vendor Defined Signal	
W2	VD_2	TBD	Vendor Defined Signal	
W10	VD_3	TBD	Vendor Defined Signal	
A1	VD_4	TBD	Vendor Defined Signal	
U5	VD_5(1)/ REFCLK_Out+ (2)	TBD/O	If the retimer supports driving REFCLK out, this pin is used for REFCLK_out+; else the pin can be used as Vendor Defined Signal	
U6	VD_6(1)/ REFCLK_Out- (2)	TBD/O	If the retimer supports driving REFCLK out, this pin is used for REFCLK_Out-; else the pin can be used as Vendor Defined Signal	
A5	VD_5	TBD	Vendor Defined Signal	
A10	VD_6	TBD	Vendor Defined Signal	
C8	VD_9	TBD	Vendor Defined Signal	
A6	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
5 pins	PWR_1	Power Rail 1	3.3 V or 1.8 V	
29 pins	PWR_2	Power Rail 2	1.1 V or 1.0 V or 0.9 V or 0.8 V	
54 pins	GND		0 V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static/ quasi static (low slew rate) signals. Routing high frequency signals on these may impose crosstalk on high-speed signals. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out, when supported is compliant with REFCLK definition in the PCIe Base Specification.

3.11.1 Signal Descriptions

3.11.1.1 SMBus Interface

Refer to Section 3.1.1.1, “SMBus Interface” on page 18.

3.11.1.2 EEPROM Interface

Refer to Section 3.1.1.2, “EEPROM Interface” on page 19

3.11.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, “Miscellaneous Signals” on page 19.

3.12 x4 Retimer Ballmap

Figure 3-10. x4 Retimer, Package-side Pin Arrangement (Top View)

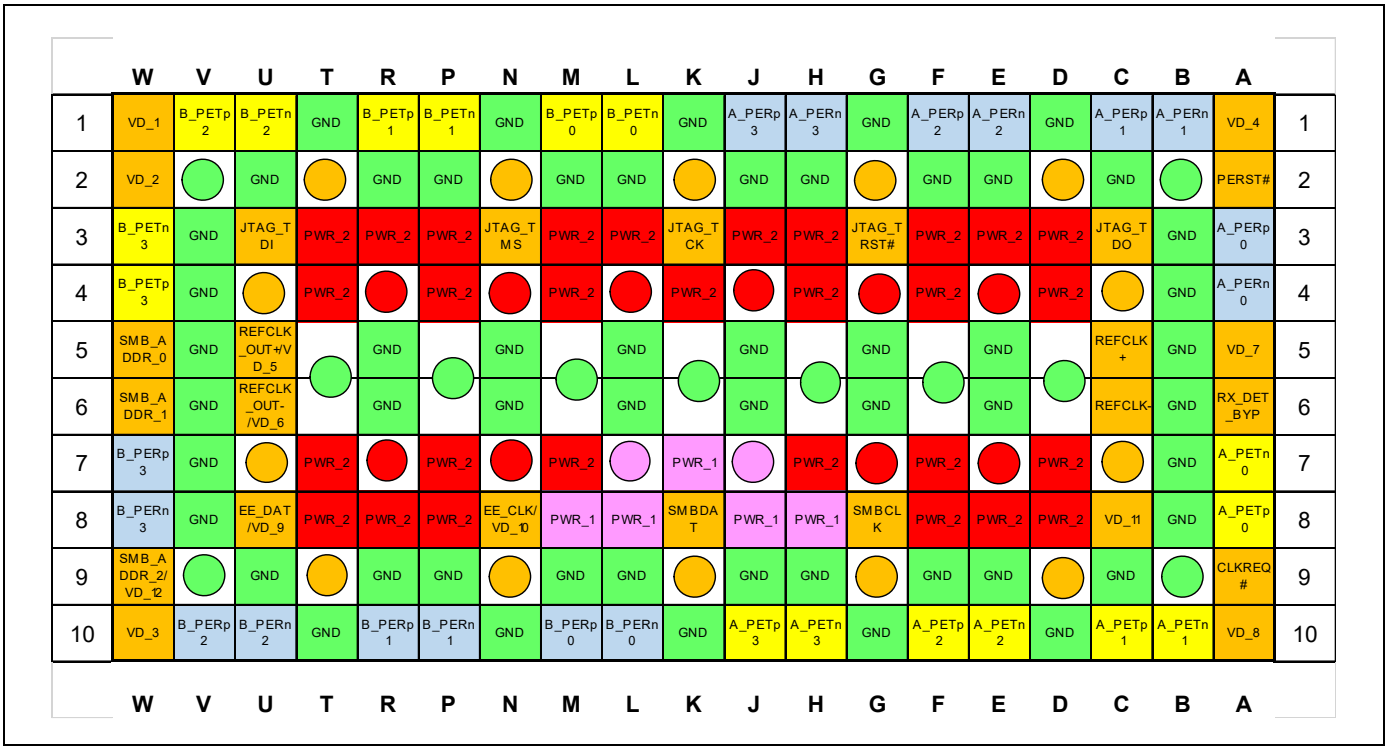
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	VD_1	B_PERp2	B_PERn2	GND	B_PERp1	B_PERn1	GND	B_PERp0	B_PERn0	GND	A_PETp3	A_PETn3	GND	A_PETp2	A_PETn2	GND	A_PETp1	A_PETn1	VD_4	1
2	VD_2		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		PERST#	2
3	B_PERn3	GND	JTAG_TDI	PWR_2	PWR_2	PWR_2	JTAG_TMS	PWR_2	PWR_2	JTAG_TCK	PWR_2	PWR_2	JTAG_TRST#	PWR_2	PWR_2	PWR_2	JTAG_TDO	GND	A_PETp0	3
4	B_PERp3	GND		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		GND	A_PETn0	4
5	SMB_ADDR_0	GND	REFCLK_OUT+/VD_5		GND		GND		GND		GND		GND		GND		REFCLK+	GND	VD_7	5
6	SMB_ADDR_1	GND	REFCLK_OUT-/VD_6		GND		GND		GND		GND		GND		GND		REFCLK-	GND	RX_DET_BYP	6
7	B_PETp3	GND		PWR_2		PWR_2		PWR_2		PWR_1		PWR_2		PWR_2		PWR_2		GND	A_PERn0	7
8	B_PETn3	GND	EE_DAT/VD_9	PWR_2	PWR_2	PWR_2	EE_CLK/VD_10	PWR_1	PWR_1	SMBDAT	PWR_1	PWR_1	SMBCLK	PWR_2	PWR_2	PWR_2	VD_11	GND	A_PERp0	8
9	SMB_ADDR_2/VD_12		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		CLKREQ#	9
10	VD_3	B_PETp2	B_PETn2	GND	B_PETp1	B_PETn1	GND	B_PETp0	B_PETn0	GND	A_PERp3	A_PERn3	GND	A_PERp2	A_PERn2	GND	A_PERp1	A_PERn1	VD_8	10
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Legend	
	PWR_1
	PWR_2
	GND
	Control Signals
	Differential TX
	Differential RX
	No Balls

3.13 x4 Retimer, Platform side Land Pattern

The following figure shows the platform side land pattern. The TX and RX balls have been swapped when compared to package side ballmap. i.e. "TX lane x" in package side ballmap gets mapped to “RX lane x” in the land pattern.

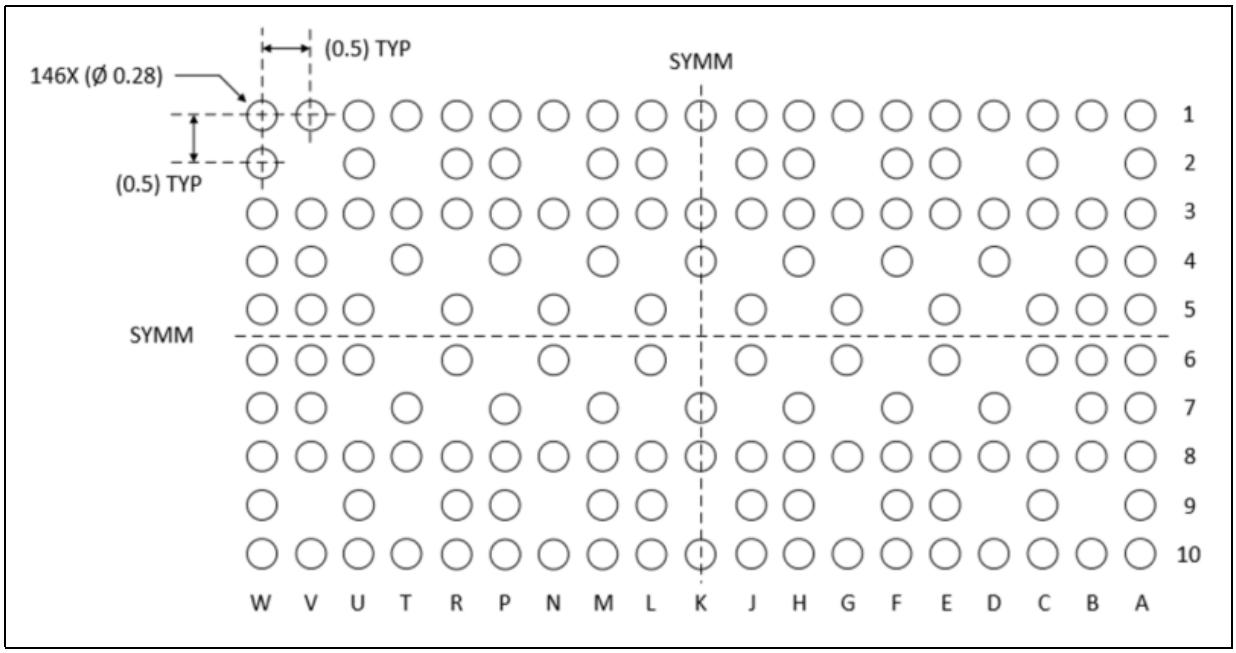
Figure 3-11. x4 Retimer, Platform-side Land Pattern (Top View)



Legend	
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via

3.14 x4 Retimer, Physical Ballmap (Package Side)

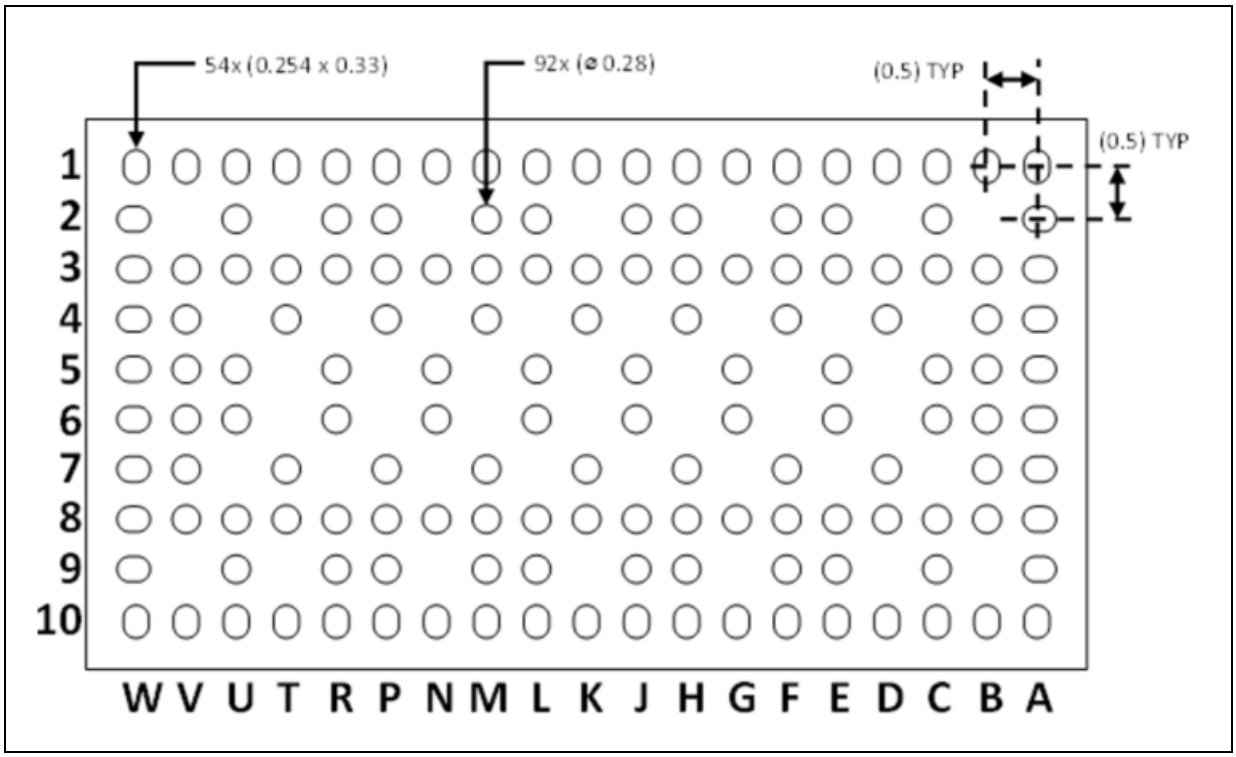
Figure 3-12. x4 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.15 X4 Retimer Platform-side Land Pattern

Figure 3-13. x4 Retimer, Platform-side Land Pattern with Spacing Details (Top View)



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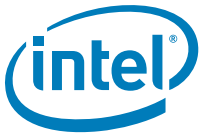


4 Electrical Characteristics

Two power supplies are supported, PWR_1 and PWR_2. PWR_1 supports 3.3 V or 1.8 V. PWR_2 supports one of (0.8 V, 0.9 V, 1.0 V, 1.1 V). Actual voltage is to be decided between retimer vendor and the system vendor.

PWR_1 rail is intended for control signals and sideband signals, whereas PWR_2 is intended for high-speed signaling.

Table 4-2 lists power distribution for the two rails (PWR_1 and PWR_2) for x4, x8 and x16 configurations.

4.1 Absolute Maximum Ratings

The following table lists the absolute maximum supply voltage ratings

Table 4-1. Absolute Maximum Voltage Ratings

Symbol	Parameter	Min	Max	Units	Notes
3.3 V	3.3 V Supply Voltage	2.8	3.6	V	1
1.8 V	1.8 V Supply Voltage	1.7	1.9	V	1
1.1 V	1.1 V Supply Voltage	1.06	1.17	V	1
1.0 V	1.0 V Supply Voltage	0.95	1.1	V	1
0.9 V	0.9 V Supply Voltage	0.86	0.98	V	1
0.8 V	0.8 V Supply Voltage	0.76	0.87	V	1

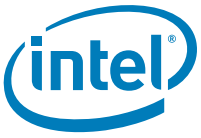
Note:
1. No specific Power-On and Power-Off sequence is required for various supply voltage rails

4.2 Power Consumption

The following table lists power consumption values under maximum operating conditions. Maximum power is consumed while all the lanes are operating at 16 GT/s with full swing on Transmitter.

Table 4-2. Recommended Absolute Maximum Power Ratings

	Power_1	Power_2	Unit
x16	1.7	6.8	W
x8	0.85	3.4	W
x4	0.425	1.7	W



4.3 Power Supply Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote upstream PCI Express device. Some basic guidelines to help ensure a quiet power supply are provided below.

Note: The following are guidelines only. It is the responsibility of the retimer designer and the platform designer to properly test the design to ensure that retimer circuitry does not create excessive noise on power supply or ground signals at the retimer package balls.

- For PWR_1 rail, a bulk decoupling capacitor of value 1x470uF (Aluminum) and 1x22uF (0805) is recommended near VR on the platform.
- For PWR_1 rail, 1x10 uF (0603) capacitor is recommended at top cavity on the platform.
- For PWR_1 rail, 1x10 uF (0603) capacitor is recommended at bottom cavity on the platform.
- For PWR_2 rail, a bulk decoupling capacitor of value 1x470 uF (Aluminum) and 1x22 uF (0805) is recommended near VR on the platform.
- For PWR_2 rail, 2x10 uF (0603) capacitors and 1x10 uF (0805) capacitor is recommended at the top cavity on the platform.
- For PWR_2 rail, 1x22 uF (0805) capacitor is recommended at the bottom cavity on the platform.
- It is recommended that the retimer vendor incorporate the decoupling caps in the package or in the die as needed to minimize noise at the package balls.

4.4 Retimer Latency

Maximum Latency (Refer to Base Specification) specification for PCIe Gen-4 retimers is 64 ns to 91 ns depending on clocking architecture and maximum payload size. Some applications may need significantly lower latency (less than 10 ns). OEMs are recommended to work with retimer vendors for this low latency use case.

4.5 Package Thermal Considerations

Parameter	Description	Value	Units
$T_{J(max)}$	Junction temperature	125	°C
$T_{A(max)}$	Ambient temperature	85	°C

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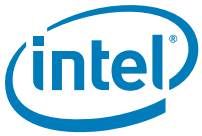

5 SMBus and EEPROM

It is assumed that each retimer has a dedicated EEPROM behind it from where the retimer loads its configuration data upon power-up. Dedicated EEPROM interface allows retimer to use fixed address to access the EEPROM.

It is recommended that the retimer load most of the configuration through EEPROM. Once the EEPROM configuration is loaded, any additional configurations needed from the platform side is done using SMBus interface. Retimer pinout supports 3 SMBus address pins allowing up to 8 addressable devices on the bus. If more than 8 devices (and hence addresses) are needed, some kind of SMBus multiplexing is used on the platform side.

Minimizing the configurations through SMBus in applications where boot time is minimized is recommended.

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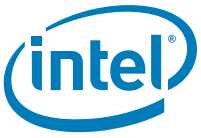
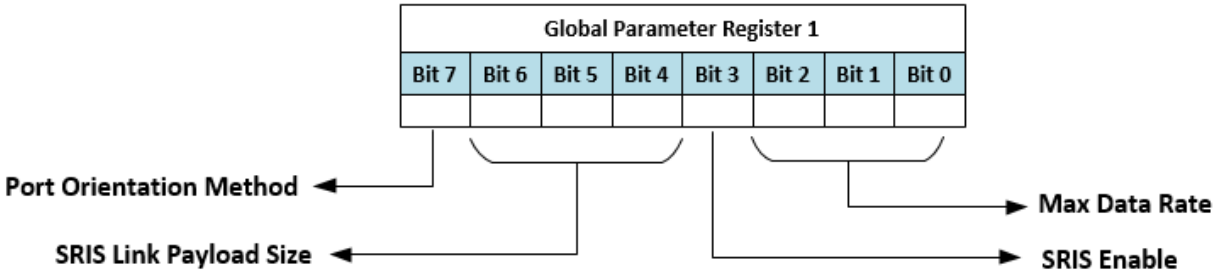


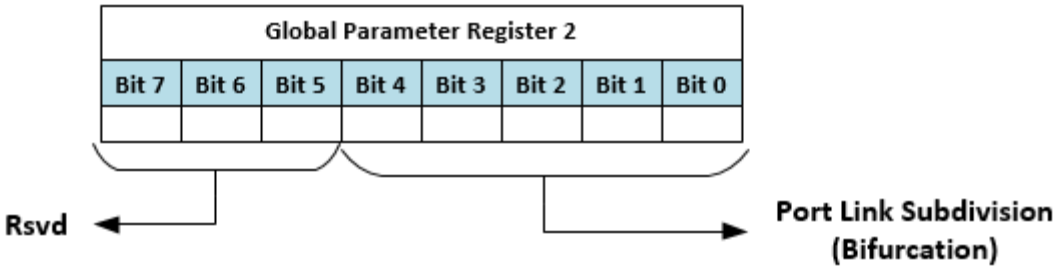
6 Register Configuration

6.1 Global Parameter Register 1



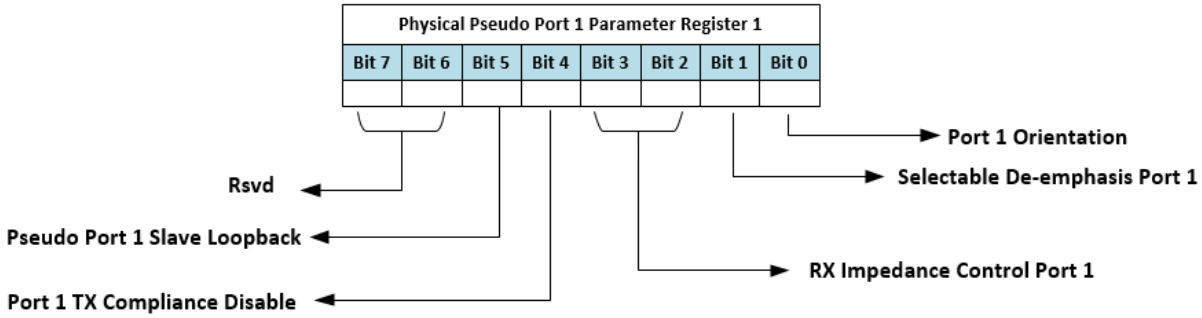
Bit Location	Register Description	Attributes
2:0	**Max Data Rate** 000: Rsvd 001: 2.5 G (Def) 010: 5.0 G 011: 8.0 G 100: 16 G 101: Rsvd 110: Rsvd	RW
3	**SRIS Enable** 0: Common Clock (Def) 1: SRIS	RW
6:4	**SRIS Link Payload Size** (valid when Bit3=1) 000: 128 001: 256 010: 512 011: 1024 100: 2048 101: 4096 (Def) 110: Rsvd 111: Rsvd	RW
7	Port Orientation Method 0:Static 1:Dynamic (Def)	RW

6.2 Global Parameter Register 2



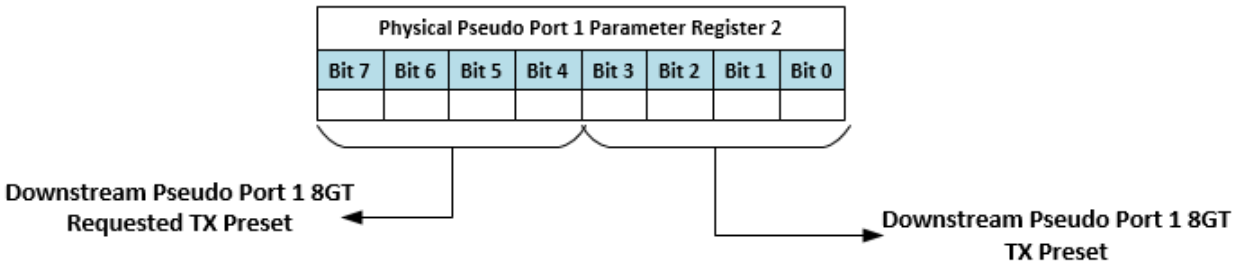
Bit Location	Register Description	Attributes
4:0	**Port Link Subdivision (Bifurcation)** 00000: x16 (Def) 00001: x8 00010: x4 00011: x8 x8 00100: x4 x4 00101: x2 x2 00110: x4 x4 x4 x4 00111: x2 x2 x2 x2 x2 x2 x2 x2 01000: x8 x4 x4 01001: x4 x2 x2 01010: x8 x4 x2 x2 01011: x2 x2 x4 01100: x4 x4 x8 01101: x2 x4 x2 01110: x2 x2x4 x8 01111-11111: Reserved	RW
7:5	Reserved	R0

6.3 Physical Pseudo Port 1 Parameter Register 1



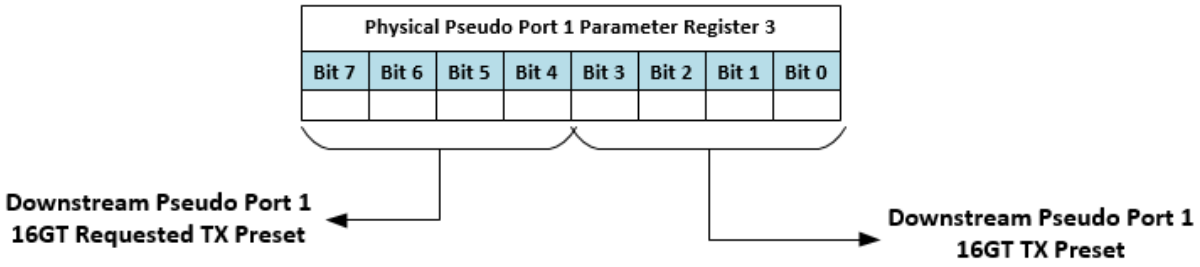
Bit Location	Register Description	Attributes
0	**Port 1 Orientation** (valid when Port Orientation Method in Global Parameter Register = 0) 0:Upstream 1: Downstream (Def)	R0
1	**Selectable De-emphasis Port 1** (valid when Port 1 Orientation =1 and Max Data Rate = 5G in Global Parameter Register) 0:-3.5 dB (Def) 1:-6.0 dB	R0
3:2	**RX Impedance Control Port 1** 00: Static- On 01: Static- Off 10: Dynamic (Def) 11: Rsvd	RW
4	**Port 1 TX Compliance Disable** 1: Disable 0: Enable (Def)	RW
5	**Pseudo Port 1 Slave Loopback** 1: Enable 0: Disable (Def)	RW
7:6	Reserved	R0

6.4 Physical Pseudo Port 1 Parameter Register 2



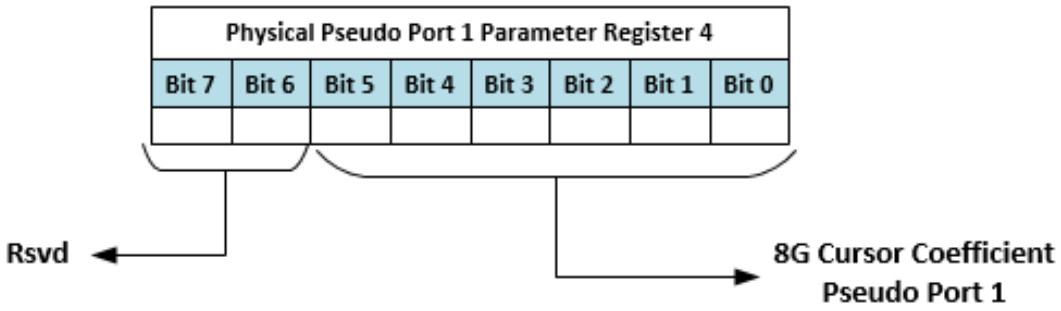
Bit Location	Register Description	Attributes
3:0	Downstream Pseudo Port 1, 8 GT/s TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	Downstream Pseudo Port 1 8 GT Requested TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW

6.5 Physical Pseudo Port 1 Parameter Register 3



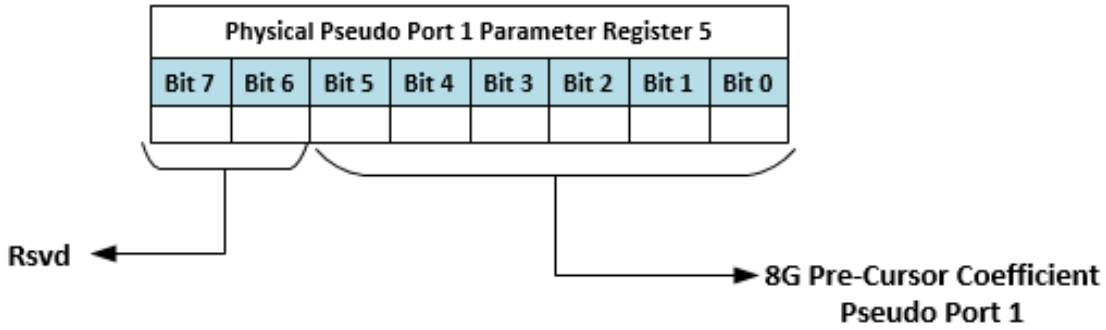
Bit Location	Register Description	Attributes
3:0	Downstream Pseudo Port 1, 16 GT/s TX Preset: 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	Downstream Pseudo Port 1 16 GT Requested TX Preset: 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW

6.6 Physical Pseudo Port 1 Parameter Register 4



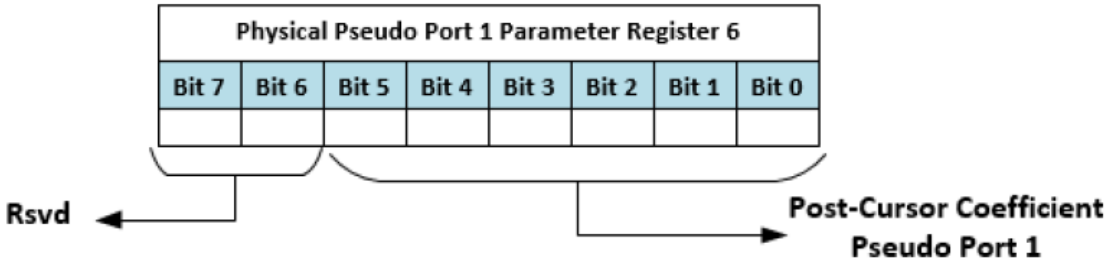
Bit Location	Register Description	Attributes
5:0	8G Cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.7 Physical Pseudo Port 1 Parameter Register 5



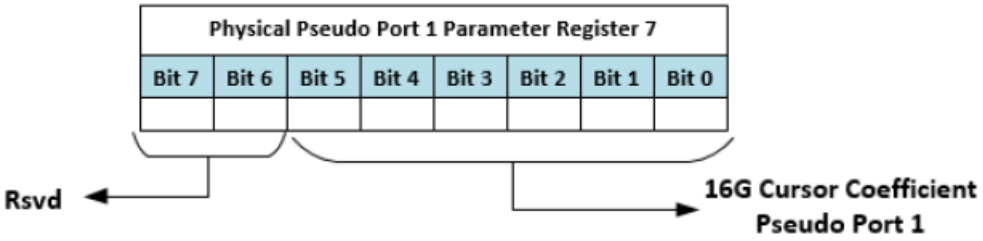
Bit Location	Register Description	Attributes
5:0	8G Pre-cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.8 Physical Pseudo Port 1 Parameter Register 6



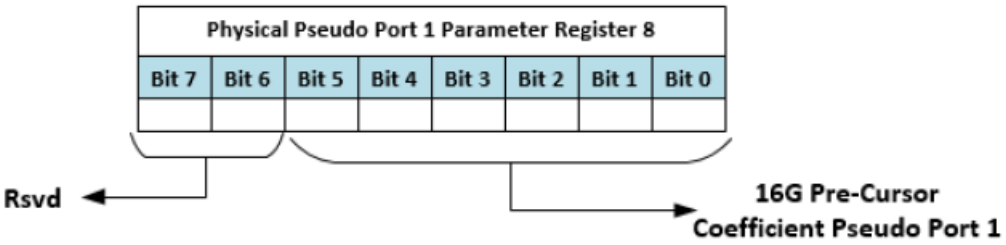
Bit Location	Register Description	Attributes
5:0	8G Post-cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.9 Physical Pseudo Port 1 Parameter Register 7



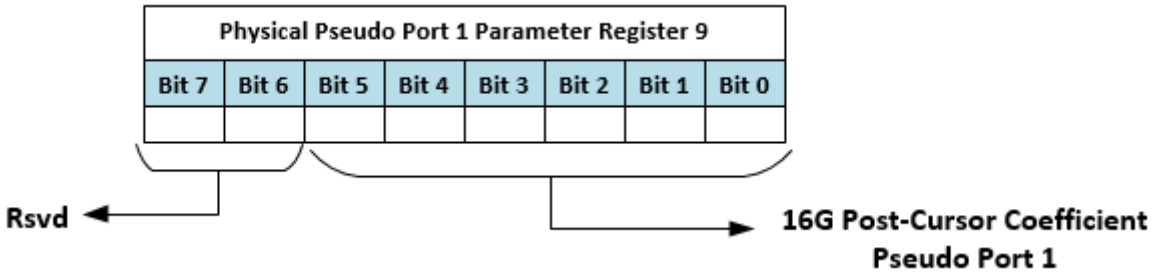
Bit Location	Register Description	Attributes
5:0	16G Cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.10 Physical Pseudo Port 1 Parameter Register 8



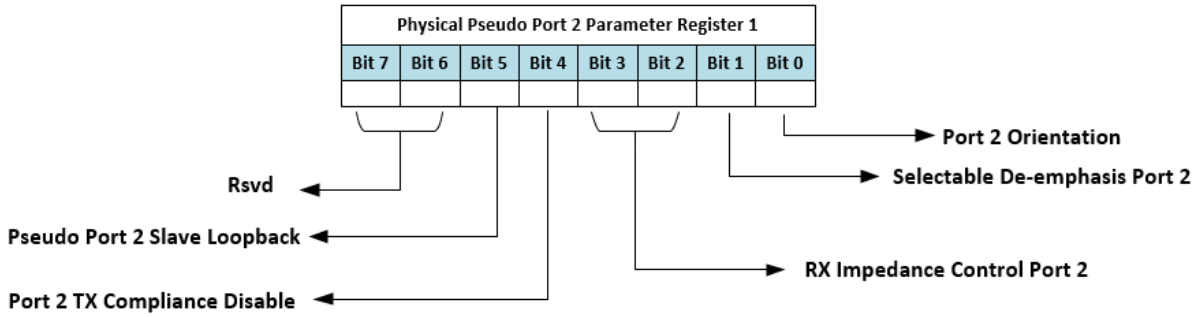
Bit Location	Register Description	Attributes
5:0	16G Pre-cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.11 Physical Pseudo Port 1 Parameter Register 9



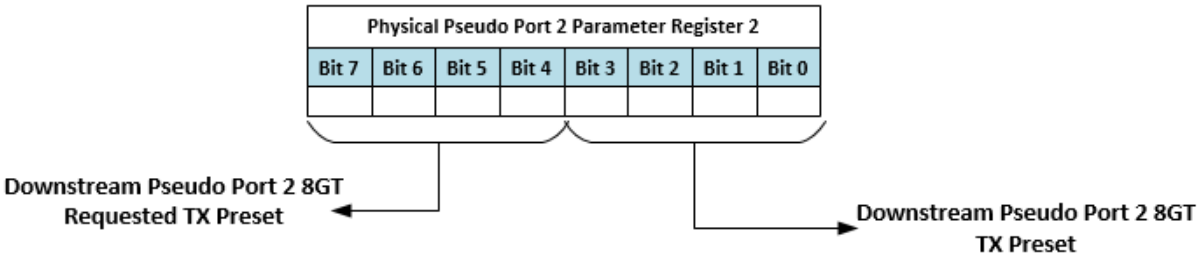
Bit Location	Register Description	Attributes
5:0	16G Post-cursor Coefficient Pseudo Port 1 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.12 Physical Pseudo Port 2 Parameter Register 1



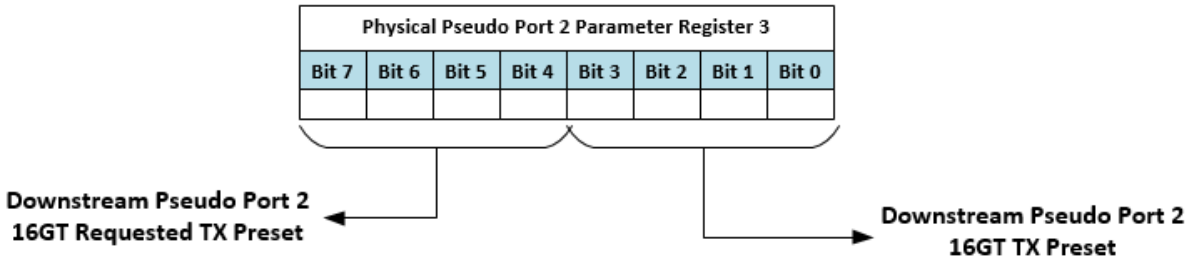
Bit Location	Register Description	Attributes
0	**Port 2 Orientation** (valid when Port Orientation Method in Global Parameter Register = 0) 0:Upstream (Def) 1:Downstream	R0
1	**Selectable De-emphasis Port 2** 0:-3.5 dB (Def) 1:-6.0 dB	R0
3:2	**RX Impedance Control Port 2** 00: Static- On 01: Static- Off 10: Dynamic (Def) 11: Rsvd	RW
4	**Port 2TX Compliance Disable** 1: Disable 0: Enable (Def)	RW
5	**Pseudo Port 2 Slave Loopback** 1: Enable 0: Disable (Def)	RW
7:6	Reserved	R0

6.13 Physical Pseudo Port 2 Parameter Register 2



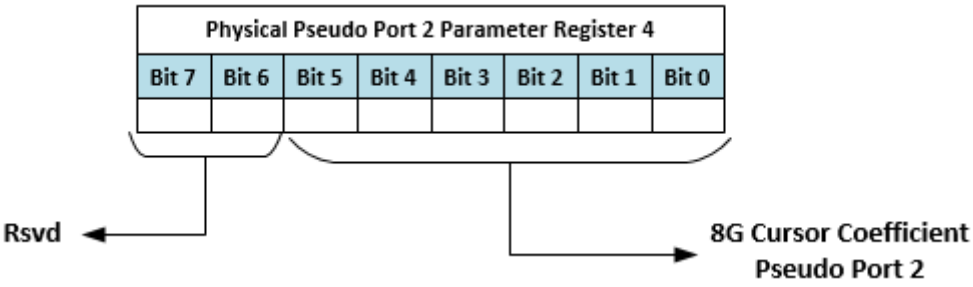
Bit Location	Register Description	Attributes
3:0	Downstream Pseudo Port 2, 8 GT/s TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	Downstream Pseudo Port 2 8GT Requested TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW

6.14 Physical Pseudo Port 2 Parameter Register 3



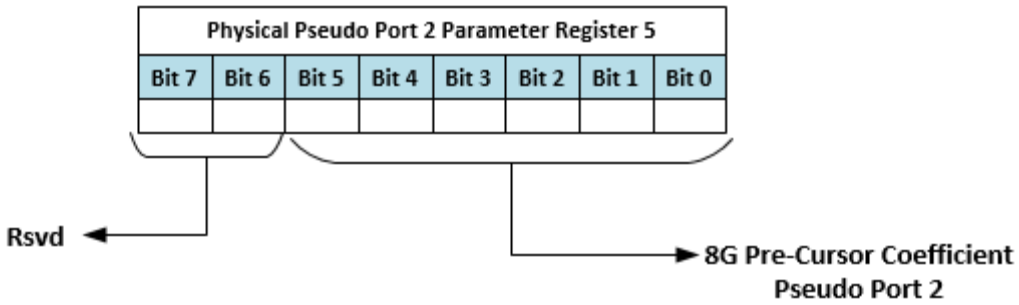
Bit Location	Register Description	Attributes
3:0	Downstream Pseudo Port 2 16 GT/s TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	Downstream Pseudo Port 2 16 GT Requested TX Preset 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW

6.15 Physical Pseudo Port 2 Parameter Register 4



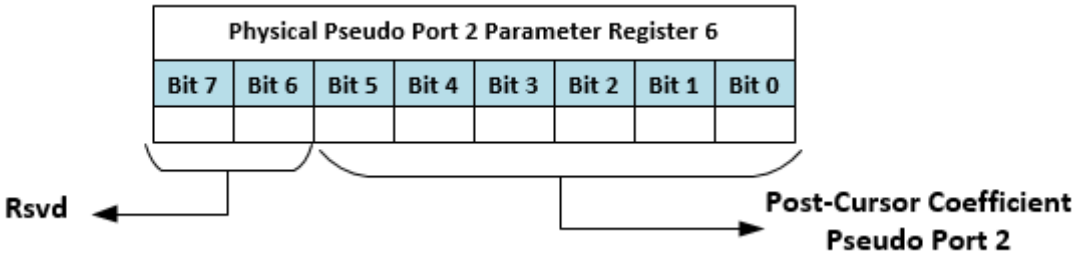
Bit Location	Register Description	Attributes
5:0	8G Cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.16 Physical Pseudo Port 2 Parameter Register 5



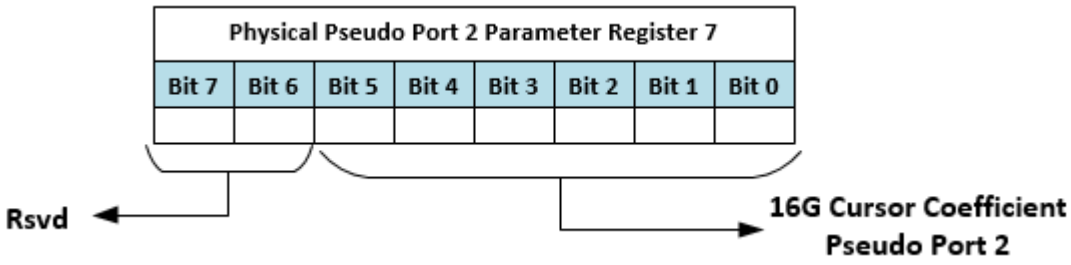
Bit Location	Register Description	Attributes
5:0	8G Pre-cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.17 Physical Pseudo Port 2 Parameter Register 6



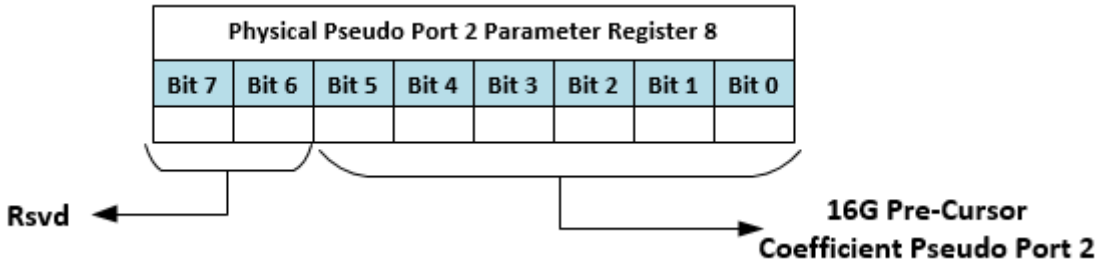
Bit Location	Register Description	Attributes
5:0	8G Post-cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.18 Physical Pseudo Port 2 Parameter Register 7



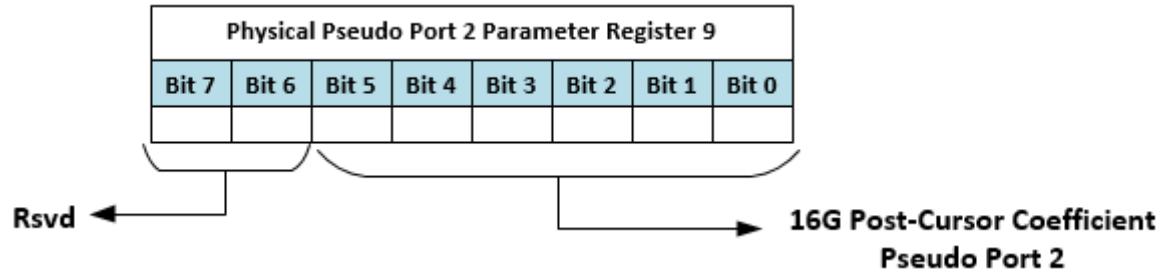
Bit Location	Register Description	Attributes
5:0	16G Cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.19 Physical Pseudo Port 2 Parameter Register 8

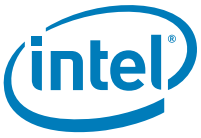


Bit Location	Register Description	Attributes
5:0	16G Pre-cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO

6.20 Physical Pseudo Port 2 Parameter Register 9



Bit Location	Register Description	Attributes
5:0	16G Post-cursor Coefficient Pseudo Port 2 Coefficient 1 to Coefficient 64	RW
7:6	Reserved	RO



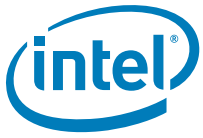
6.21 Register Offsets for Different Link Subdivision (Bifurcation)

The following table shows register offsets for various port bifurcation schemes.

Table 6-1. Register Offsets

	Offset	Link subdivision						
	x16, x8, x4							
	x8	x8						
	x4	x4						
	x2	x2						
	x4	x4	x4	x4				
	x2	x2	x2	x2				
	x2	x2	x2	x2	x2	x2	x2	x2
Global Parameter Register 1	0x00							
Global Parameter Register 2	0x01							
Physical Pseudo Port 1 Parameter Register 1	0x02	0x14	0x26	0x38	0x4A	0x5C	0x6E	0x81
Physical Pseudo Port 1 Parameter Register 2	0x03	0x15	0x27	0x39	0x4B	0x5D	0x6F	0x82
Physical Pseudo Port 1 Parameter Register 3	0x04	0x16	0x28	0x3A	0x4C	0x5E	0x71	0x83
Physical Pseudo Port 1 Parameter Register 4	0x05	0x17	0x29	0x3B	0x4D	0x5F	0x72	0x84
Physical Pseudo Port 1 Parameter Register 5	0x06	0x18	0x2A	0x3C	0x4E	0x60	0x73	0x85
Physical Pseudo Port 1 Parameter Register 6	0x07	0x19	0x2B	0x3D	0x4F	0x61	0x74	0x86
Physical Pseudo Port 1 Parameter Register 7	0x08	0x1A	0x2C	0x3E	0x50	0x62	0x75	0x87
Physical Pseudo Port 1 Parameter Register 8	0x09	0x1B	0x2D	0x3F	0x51	0x63	0x76	0x88
Physical Pseudo Port 1 Parameter Register 9	0x0A	0x1C	0x2E	0x40	0x52	0x64	0x77	0x89
Physical Pseudo Port 2 Parameter Register 1	0x0B	0x1D	0x2F	0x41	0x53	0x65	0x78	0x8A
Physical Pseudo Port 2 Parameter Register 2	0x0C	0x1E	0x30	0x42	0x54	0x66	0x79	0x8B
Physical Pseudo Port 2 Parameter Register 3	0x0D	0x1F	0x31	0x43	0x55	0x67	0x7A	0x8C
Physical Pseudo Port 2 Parameter Register 4	0x0E	0x20	0x32	0x44	0x56	0x68	0x7B	0x8D
Physical Pseudo Port 2 Parameter Register 5	0x0F	0x21	0x33	0x45	0x57	0x69	0x7C	0x8E
Physical Pseudo Port 2 Parameter Register 6	0x10	0x22	0x34	0x46	0x58	0x6A	0x7D	0x8F
Physical Pseudo Port 2 Parameter Register 7	0x11	0x23	0x35	0x47	0x59	0x6B	0x7E	0x90
Physical Pseudo Port 2 Parameter Register 8	0x12	0x24	0x36	0x48	0x5A	0x6C	0x7F	0x91
Physical Pseudo Port 2 Parameter Register 9	0x13	0x25	0x37	0x49	0x5B	0x6D	0x80	0x92

There will be one instance of all 20 registers when the port is used as x16, x8 or x4 with no link sub-division. When link subdivision is used, the number of pseudo port registers gets multiplied by the number of subdivided links. Table above shows that the maximum number of registers will be used when the x16 link is subdivided as 8 x2. The number of registers needed may be different depending on whether sub divided links share the register settings or not.



6.22 Register Bit Level Details

Table 6-2. Register Bit Level Details (Sheet 1 of 17)

Global Parameter Register 1	1	x	x	x	x	x	x	x	Dynamic Port Orientation
	0	x	x	x	x	x	x	x	Static Port Orientation
	x	x	0	0	0	x	x	x	SRIS Max Payload Size=128 Bytes (Valid for SRIS Enable only)
	x	x	0	0	1	x	x	x	SRIS Max Payload Size=256 Bytes (Valid for SRIS Enable only)
	x	x	0	1	0	x	x	x	SRIS Max Payload Size=512 Bytes (Valid for SRIS Enable only)
	x	x	0	1	1	x	x	x	SRIS Max Payload Size=1024 Bytes (Valid for SRIS Enable only)
	x	x	1	0	0	x	x	x	SRIS Max Payload Size=2048 Bytes (Valid for SRIS Enable only)
	x	x	1	0	1	x	x	x	SRIS Max Payload Size=4096 Bytes (Valid for SRIS Enable only)
	x	x	1	1	0	x	x	x	Rsvd Max payload
	x	x	1	1	1	x	x	x	Rsvd Max payload
	x	x	x	x	1	x	x	x	SRIS Enable
	x	x	x	x	0	x	x	x	Common Clock Enable
	x	x	x	x	x	0	0	0	Rsvd Max Data Rate
	x	x	x	x	x	0	0	1	Max Data Rate 2.5 G
	x	x	x	x	x	0	1	0	Max Data Rate 5 G
	x	x	x	x	x	0	1	1	Max Data Rate 8 G
	x	x	x	x	x	1	0	0	Max Data Rate 16 G
	x	x	x	x	x	1	0	1	Rsvd Max Data Rate
	x	x	x	x	x	1	1	0	Rsvd Max Data Rate
	x	x	x	x	x	1	1	1	Rsvd Max Data Rate
Global Parameter Register 2	x	x	x	0	0	0	0	0	x16
	x	x	x	0	0	0	0	1	x8
	x	x	x	0	0	0	1	0	x4
	x	x	x	0	0	0	1	1	x8 x8
	x	x	x	0	0	1	0	0	x4 x4
	x	x	x	0	0	1	0	1	x2 x2
	x	x	x	0	0	1	1	0	x4 x4 x4 x4
	x	x	x	0	0	1	1	1	x2 x2 x2 x2 x2 x2 x2 x2
	x	x	x	0	1	0	0	0	x8 x4 x4
	x	x	x	0	1	0	0	1	x4 x2 x2
	x	x	x	0	1	0	1	0	x8 x4 x2 x2
	x	x	x	0	1	0	1	1	x2 x2 x4
	x	x	x	0	1	1	0	0	x4 x4 x8
	x	x	x	0	1	1	0	1	x2 x4 x2
	x	x	x	0	1	1	1	0	x2 x2 x4 x8
	x	x	x	0	1	1	1	1	Rsvd Bifurcation
	x	x	x	1	0	0	0	0	Rsvd Bifurcation
	x	x	x	1	0	0	0	1	Rsvd Bifurcation
	x	x	x	1	0	0	1	0	Rsvd Bifurcation
	x	x	x	1	0	0	1	1	Rsvd Bifurcation
	x	x	x	1	0	1	0	0	Rsvd Bifurcation
	x	x	x	1	0	1	0	1	Rsvd Bifurcation
	x	x	x	1	0	1	1	0	Rsvd Bifurcation
	x	x	x	1	0	1	1	1	Rsvd Bifurcation
	x	x	x	1	1	0	0	0	Rsvd Bifurcation
	x	x	x	1	1	0	0	1	Rsvd Bifurcation
	x	x	x	1	1	0	1	0	Rsvd Bifurcation
	x	x	x	1	1	0	1	1	Rsvd Bifurcation
	x	x	x	1	1	1	0	0	Rsvd Bifurcation
	x	x	x	1	1	1	0	1	Rsvd Bifurcation
	x	x	x	1	1	1	1	0	Rsvd Bifurcation
	x	x	x	1	1	1	1	1	Rsvd Bifurcation

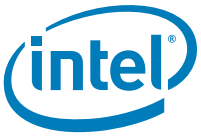


Table 6-2 Register Bit Level Details (Sheet 2 of 17)

Physical Pseudo Port 1 Parameter Register 1	x	x	x	x	x	x	x	0	Pseudo Port 1 Orientation Method- Upstream
	x	x	x	x	x	x	x	1	Pseudo Port 1 Orientation Method- Downstream
	x	x	x	x	x	x	0	x	Selectable De-emphasis Port1-> -3.5dB
	x	x	x	x	x	x	1	x	Selectable De-emphasis Port1-> -6.0dB
	x	x	x	x	0	0	x	x	Pseudo Port 1 RX Impedance Control-Static On
	x	x	x	x	0	1	x	x	Pseudo Port 1 RX Impedance Control-Static Off
	x	x	x	x	1	0	x	x	Pseudo Port 1 RX Impedance Control-Dynamic
	x	x	x	x	1	1	x	x	Pseudo Port 1 RX Impedance Control-Rsvd
	x	x	x	0	x	x	x	x	Pseudo Port 1 TX Compliance Enable
	x	x	x	1	x	x	x	x	Pseudo Port 1 TX Compliance Disable
	x	x	1	x	x	x	x	x	Pseudo Port 1 TX Slave Loopback Enable
	x	x	0	x	x	x	x	x	Pseudo Port 1 TX Slave Loopback Disable
	0	0	x	x	x	x	x	x	Rsvd
	0	1	x	x	x	x	x	x	Rsvd
	1	0	x	x	x	x	x	x	Rsvd
	1	1	x	x	x	x	x	x	Rsvd
Physical Pseudo Port 1 Parameter Register 2	x	x	x	x	0	0	0	0	Downstream Pseudo Port 1 TX Preset_0 @8G
	x	x	x	x	0	0	0	1	Downstream Pseudo Port 1 TX Preset_1 @8G
	x	x	x	x	0	0	1	0	Downstream Pseudo Port 1 TX Preset_2 @8G
	x	x	x	x	0	0	1	1	Downstream Pseudo Port 1 TX Preset_3@8G
	x	x	x	x	0	1	0	0	Downstream Pseudo Port 1 TX Preset_4 @8G
	x	x	x	x	0	1	0	1	Downstream Pseudo Port 1 TX Preset_5 @8G
	x	x	x	x	0	1	1	0	Downstream Pseudo Port 1 TX Preset_6 @8G
	x	x	x	x	0	1	1	1	Downstream Pseudo Port 1 TX Preset_7 @8G
	x	x	x	x	1	0	0	0	Downstream Pseudo Port 1 TX Preset_8 @8G
	x	x	x	x	1	0	0	1	Downstream Pseudo Port 1 TX Preset_9 @8G
	x	x	x	x	1	0	1	0	Downstream Pseudo Port 1 TX Preset_10 @8G
	x	x	x	x	1	0	1	1	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	0	0	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	0	1	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	1	0	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	1	1	Downstream Pseudo Port 1 TX Preset Rsvd
	0	0	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_0 @8G
	0	0	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_1 @8G
	0	0	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_2 @8G
	0	0	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_3@8G
	0	1	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_4 @8G
	0	1	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_5 @8G
	0	1	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_6 @8G
	0	1	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_7 @8G
	1	0	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_8 @8G
	1	0	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_9 @8G
	1	0	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_10 @8G
	1	0	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd

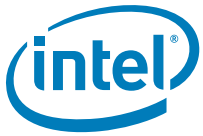


Table 6-2 Register Bit Level Details (Sheet 3 of 17)

Physical Pseudo Port 1 Parameter Register 3	x	x	x	x	0	0	0	0	Downstream Pseudo Port 1 TX Preset_0 @16G
	x	x	x	x	0	0	0	1	Downstream Pseudo Port 1 TX Preset_1 @16G
	x	x	x	x	0	0	1	0	Downstream Pseudo Port 1 TX Preset_2 @16G
	x	x	x	x	0	0	1	1	Downstream Pseudo Port 1 TX Preset_3@16G
	x	x	x	x	0	1	0	0	Downstream Pseudo Port 1 TX Preset_4 @16G
	x	x	x	x	0	1	0	1	Downstream Pseudo Port 1 TX Preset_5 @16G
	x	x	x	x	0	1	1	0	Downstream Pseudo Port 1 TX Preset_6 @16G
	x	x	x	x	0	1	1	1	Downstream Pseudo Port 1 TX Preset_7 @16G
	x	x	x	x	1	0	0	0	Downstream Pseudo Port 1 TX Preset_8 @16G
	x	x	x	x	1	0	0	1	Downstream Pseudo Port 1 TX Preset_9 @16G
	x	x	x	x	1	0	1	0	Downstream Pseudo Port 1 TX Preset_10 @16G
	x	x	x	x	1	0	1	1	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	0	0	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	0	1	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	1	0	Downstream Pseudo Port 1 TX Preset Rsvd
	x	x	x	x	1	1	1	1	Downstream Pseudo Port 1 TX Preset Rsvd
	0	0	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_0 @16G
	0	0	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_1 @16G
	0	0	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_2 @16G
	0	0	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_3@16G
	0	1	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_4 @16G
	0	1	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_5 @16G
	0	1	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_6 @16G
	0	1	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_7 @16G
	1	0	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_8 @16G
	1	0	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_9 @16G
	1	0	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset_10 @16G
	1	0	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	0	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	0	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	1	0	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd
	1	1	1	1	x	x	x	x	Downstream Pseudo Port 1 Requested TX Preset Rsvd

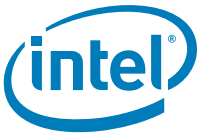


Table 6-2 Register Bit Level Details (Sheet 4 of 17)

Physical Pseudo Port 1 Parameter Register 4	x	x	0	0	0	0	0	0	Cursor Coefficient 1 Psuedo Port 1
8G	x	x	0	0	0	0	0	1	Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Cursor Coefficient 64 Psuedo Port 1

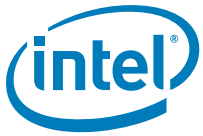


Table 6-2 Register Bit Level Details (Sheet 5 of 17)

Physical Pseudo Port 1 Parameter Register 5	x	x	0	0	0	0	0	0	Pre-Cursor Coefficient 1 Psuedo Port 1
8G	x	x	0	0	0	0	0	1	Pre-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Pre-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Pre-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Pre-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Pre-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Pre-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Pre-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Pre-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Pre-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Pre-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Pre-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Pre-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Pre-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Pre-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Pre-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Pre-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Pre-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Pre-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Pre-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Pre-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Pre-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Pre-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Pre-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Pre-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Pre-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Pre-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Pre-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Pre-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Pre-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Pre-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Pre-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Pre-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Pre-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Pre-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Pre-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Pre-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Pre-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Pre-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Pre-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Pre-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Pre-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Pre-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Pre-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Pre-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Pre-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Pre-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Pre-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Pre-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Pre-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Pre-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Pre-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Pre-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Pre-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Pre-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Pre-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Pre-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Pre-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Pre-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Pre-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Pre-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Pre-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Pre-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Pre-Cursor Coefficient 64 Psuedo Port 1

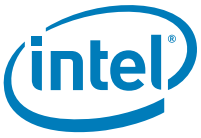


Table 6-2 Register Bit Level Details (Sheet 6 of 17)

Physical Pseudo Port 1 Parameter Register 6	x	x	0	0	0	0	0	0	Post-Cursor Coefficient 1 Psuedo Port 1
8G	x	x	0	0	0	0	0	1	Post-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Post-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Post-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Post-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Post-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Post-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Post-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Post-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Post-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Post-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Post-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Post-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Post-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Post-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Post-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Post-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Post-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Post-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Post-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Post-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Post-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Post-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Post-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Post-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Post-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Post-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Post-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Post-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Post-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Post-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Post-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Post-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Post-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Post-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Post-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Post-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Post-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Post-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Post-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Post-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Post-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Post-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Post-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Post-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Post-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Post-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Post-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Post-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Post-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Post-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Post-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Post-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Post-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Post-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Post-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Post-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Post-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Post-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Post-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Post-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Post-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Post-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Post-Cursor Coefficient 64 Psuedo Port 1

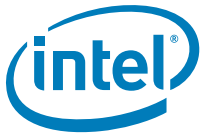


Table 6-2 Register Bit Level Details (Sheet 7 of 17)

Physical Pseudo Port 1 Parameter Register 7	x	x	0	0	0	0	0	0	Cursor Coefficient 1 Psuedo Port 1
16G	x	x	0	0	0	0	0	1	Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Cursor Coefficient 64 Psuedo Port 1

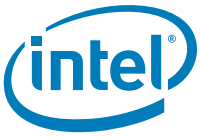


Table 6-2 Register Bit Level Details (Sheet 8 of 17)

Physical Pseudo Port 1 Parameter Register 8	x	x	0	0	0	0	0	0	Pre-Cursor Coefficient 1 Psuedo Port 1
16G	x	x	0	0	0	0	0	1	Pre-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Pre-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Pre-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Pre-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Pre-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Pre-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Pre-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Pre-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Pre-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Pre-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Pre-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Pre-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Pre-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Pre-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Pre-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Pre-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Pre-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Pre-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Pre-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Pre-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Pre-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Pre-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Pre-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Pre-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Pre-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Pre-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Pre-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Pre-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Pre-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Pre-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Pre-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Pre-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Pre-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Pre-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Pre-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Pre-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Pre-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Pre-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Pre-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Pre-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Pre-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Pre-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Pre-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Pre-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Pre-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Pre-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Pre-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Pre-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Pre-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Pre-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Pre-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Pre-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Pre-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Pre-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Pre-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Pre-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Pre-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Pre-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Pre-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Pre-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Pre-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Pre-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Pre-Cursor Coefficient 64 Psuedo Port 1

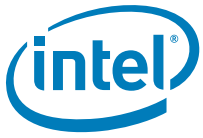


Table 6-2 Register Bit Level Details (Sheet 9 of 17)

Physical Pseudo Port 1 Parameter Register 9	x	x	0	0	0	0	0	0	Post-Cursor Coefficient 1 Psuedo Port 1
	x	x	0	0	0	0	0	1	Post-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Post-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Post-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Post-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Post-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Post-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Post-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Post-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Post-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Post-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Post-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Post-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Post-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Post-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Post-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Post-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Post-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Post-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Post-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Post-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Post-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Post-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Post-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Post-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Post-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Post-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Post-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Post-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Post-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Post-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Post-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Post-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Post-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Post-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Post-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Post-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Post-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Post-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Post-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Post-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Post-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Post-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Post-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Post-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Post-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Post-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Post-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Post-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Post-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Post-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Post-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Post-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Post-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Post-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Post-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Post-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Post-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Post-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Post-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Post-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Post-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Post-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Post-Cursor Coefficient 64 Psuedo Port 1

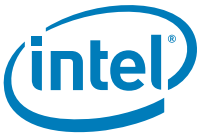


Table 6-2 Register Bit Level Details (Sheet 10 of 17)

Physical Pseudo Port 2 Parameter Register 1	x	x	x	x	x	x	x	0	Pseudo Port 2 Orientation Method- Upstream
	x	x	x	x	x	x	x	1	Pseudo Port 2 Orientation Method- Downstream
	x	x	x	x	x	x	0	x	Selectable De-emphasis Port1-> -3.5dB
	x	x	x	x	x	x	1	x	Selectable De-emphasis Port1-> -6.0dB
	x	x	x	x	0	0	x	x	Pseudo Port 2 RX Impedance Control-Static On
	x	x	x	x	0	1	x	x	Pseudo Port 2 RX Impedance Control-Static Off
	x	x	x	x	1	0	x	x	Pseudo Port 2 RX Impedance Control-Dynamic
	x	x	x	x	1	1	x	x	Pseudo Port 2 RX Impedance Control-Rsvd
	x	x	x	0	x	x	x	x	Pseudo Port 2 TX Compliance Enable
	x	x	x	1	x	x	x	x	Pseudo Port 2 TX Compliance Disable
	x	x	1	x	x	x	x	x	Pseudo Port 2 TX Slave Loopback Enable
	x	x	0	x	x	x	x	x	Pseudo Port 2 TX Slave Loopback Disable
	0	0	x	x	x	x	x	x	Rsvd
	0	1	x	x	x	x	x	x	Rsvd
	1	0	x	x	x	x	x	x	Rsvd
	1	1	x	x	x	x	x	x	Rsvd
Physical Pseudo Port 2 Parameter Register 2	x	x	x	x	0	0	0	0	Downstream Pseudo Port 2 TX Preset_0 @8G
	x	x	x	x	0	0	0	1	Downstream Pseudo Port 2 TX Preset_1 @8G
	x	x	x	x	0	0	1	0	Downstream Pseudo Port 2 TX Preset_2 @8G
	x	x	x	x	0	0	1	1	Downstream Pseudo Port 2 TX Preset_3@8G
	x	x	x	x	0	1	0	0	Downstream Pseudo Port 2 TX Preset_4 @8G
	x	x	x	x	0	1	0	1	Downstream Pseudo Port 2 TX Preset_5 @8G
	x	x	x	x	0	1	1	0	Downstream Pseudo Port 2 TX Preset_6 @8G
	x	x	x	x	0	1	1	1	Downstream Pseudo Port 2 TX Preset_7 @8G
	x	x	x	x	1	0	0	0	Downstream Pseudo Port 2 TX Preset_8 @8G
	x	x	x	x	1	0	0	1	Downstream Pseudo Port 2 TX Preset_9 @8G
	x	x	x	x	1	0	1	0	Downstream Pseudo Port 2 TX Preset_10 @8G
	x	x	x	x	1	0	1	1	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	0	0	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	0	1	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	1	0	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	1	1	Downstream Pseudo Port 2 TX Preset Rsvd
	0	0	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_0 @8G
	0	0	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_1 @8G
	0	0	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_2 @8G
	0	0	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_3@8G
	0	1	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_4 @8G
	0	1	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_5 @8G
	0	1	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_6 @8G
	0	1	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_7 @8G
	1	0	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_8 @8G
	1	0	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_9 @8G
	1	0	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_10 @8G
	1	0	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd

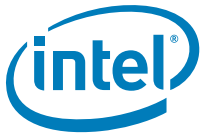


Table 6-2 Register Bit Level Details (Sheet 11 of 17)

Physical Pseudo Port 2 Parameter Register 3	x	x	x	x	0	0	0	0	Downstream Pseudo Port 2 TX Preset_0 @16G
	x	x	x	x	0	0	0	1	Downstream Pseudo Port 2 TX Preset_1 @16G
	x	x	x	x	0	0	1	0	Downstream Pseudo Port 2 TX Preset_2 @16G
	x	x	x	x	0	0	1	1	Downstream Pseudo Port 2 TX Preset_3@16G
	x	x	x	x	0	1	0	0	Downstream Pseudo Port 2 TX Preset_4 @16G
	x	x	x	x	0	1	0	1	Downstream Pseudo Port 2 TX Preset_5 @16G
	x	x	x	x	0	1	1	0	Downstream Pseudo Port 2 TX Preset_6 @16G
	x	x	x	x	0	1	1	1	Downstream Pseudo Port 2 TX Preset_7 @16G
	x	x	x	x	1	0	0	0	Downstream Pseudo Port 2 TX Preset_8 @16G
	x	x	x	x	1	0	0	1	Downstream Pseudo Port 2 TX Preset_9 @16G
	x	x	x	x	1	0	1	0	Downstream Pseudo Port 2 TX Preset_10 @16G
	x	x	x	x	1	0	1	1	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	0	0	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	0	1	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	1	0	Downstream Pseudo Port 2 TX Preset Rsvd
	x	x	x	x	1	1	1	1	Downstream Pseudo Port 2 TX Preset Rsvd
	0	0	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_0 @16G
	0	0	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_1 @16G
	0	0	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_2 @16G
	0	0	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_3@16G
	0	1	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_4 @16G
	0	1	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_5 @16G
	0	1	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_6 @16G
	0	1	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_7 @16G
	1	0	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_8 @16G
	1	0	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_9 @16G
	1	0	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset_10 @16G
	1	0	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	0	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	0	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	1	0	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd
	1	1	1	1	x	x	x	x	Downstream Pseudo Port 2 Requested TX Preset Rsvd

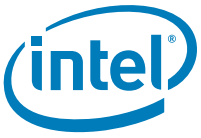


Table 6-2 Register Bit Level Details (Sheet 12 of 17)

Physical Pseudo Port 2 Parameter Register 4	x	x	0	0	0	0	0	0	Cursor Coefficient 1 Psuedo Port 2
	x	x	0	0	0	0	0	1	Cursor Coefficient 2 Psuedo Port 2
	x	x	0	0	0	0	1	0	Cursor Coefficient 3 Psuedo Port 2
	x	x	0	0	0	0	1	1	Cursor Coefficient 4 Psuedo Port 2
	x	x	0	0	0	1	0	0	Cursor Coefficient 5 Psuedo Port 2
	x	x	0	0	0	1	0	1	Cursor Coefficient 6 Psuedo Port 2
	x	x	0	0	0	1	1	0	Cursor Coefficient 7 Psuedo Port 2
	x	x	0	0	0	1	1	1	Cursor Coefficient 8 Psuedo Port 2
	x	x	0	0	1	0	0	0	Cursor Coefficient 9 Psuedo Port 2
	x	x	0	0	1	0	0	1	Cursor Coefficient 10 Psuedo Port 2
	x	x	0	0	1	0	1	0	Cursor Coefficient 11 Psuedo Port 2
	x	x	0	0	1	0	1	1	Cursor Coefficient 12 Psuedo Port 2
	x	x	0	0	1	1	0	0	Cursor Coefficient 13 Psuedo Port 2
	x	x	0	0	1	1	0	1	Cursor Coefficient 14 Psuedo Port 2
	x	x	0	0	1	1	1	0	Cursor Coefficient 15 Psuedo Port 2
	x	x	0	0	1	1	1	1	Cursor Coefficient 16 Psuedo Port 2
	x	x	0	1	0	0	0	0	Cursor Coefficient 17 Psuedo Port 2
	x	x	0	1	0	0	0	1	Cursor Coefficient 18 Psuedo Port 2
	x	x	0	1	0	0	1	0	Cursor Coefficient 19 Psuedo Port 2
	x	x	0	1	0	0	1	1	Cursor Coefficient 20 Psuedo Port 2
	x	x	0	1	0	1	0	0	Cursor Coefficient 21 Psuedo Port 2
	x	x	0	1	0	1	0	1	Cursor Coefficient 22 Psuedo Port 2
	x	x	0	1	0	1	1	0	Cursor Coefficient 23 Psuedo Port 2
	x	x	0	1	0	1	1	1	Cursor Coefficient 24 Psuedo Port 2
	x	x	0	1	1	0	0	0	Cursor Coefficient 25 Psuedo Port 2
	x	x	0	1	1	0	0	1	Cursor Coefficient 26 Psuedo Port 2
	x	x	0	1	1	0	1	0	Cursor Coefficient 27 Psuedo Port 2
	x	x	0	1	1	0	1	1	Cursor Coefficient 28 Psuedo Port 2
	x	x	0	1	1	1	0	0	Cursor Coefficient 29 Psuedo Port 2
	x	x	0	1	1	1	0	1	Cursor Coefficient 30 Psuedo Port 2
	x	x	0	1	1	1	1	0	Cursor Coefficient 31 Psuedo Port 2
	x	x	0	1	1	1	1	1	Cursor Coefficient 32 Psuedo Port 2
	x	x	1	0	0	0	0	0	Cursor Coefficient 33 Psuedo Port 2
	x	x	1	0	0	0	0	1	Cursor Coefficient 34 Psuedo Port 2
	x	x	1	0	0	0	1	0	Cursor Coefficient 35 Psuedo Port 2
	x	x	1	0	0	0	1	1	Cursor Coefficient 36 Psuedo Port 2
	x	x	1	0	0	1	0	0	Cursor Coefficient 37 Psuedo Port 2
	x	x	1	0	0	1	0	1	Cursor Coefficient 38 Psuedo Port 2
	x	x	1	0	0	1	1	0	Cursor Coefficient 39 Psuedo Port 2
	x	x	1	0	0	1	1	1	Cursor Coefficient 40 Psuedo Port 2
	x	x	1	0	1	0	0	0	Cursor Coefficient 41 Psuedo Port 2
	x	x	1	0	1	0	0	1	Cursor Coefficient 42 Psuedo Port 2
	x	x	1	0	1	0	1	0	Cursor Coefficient 43 Psuedo Port 2
	x	x	1	0	1	0	1	1	Cursor Coefficient 44 Psuedo Port 2
	x	x	1	0	1	1	0	0	Cursor Coefficient 45 Psuedo Port 2
	x	x	1	0	1	1	0	1	Cursor Coefficient 46 Psuedo Port 2
	x	x	1	0	1	1	1	0	Cursor Coefficient 47 Psuedo Port 2
	x	x	1	0	1	1	1	1	Cursor Coefficient 48 Psuedo Port 2
	x	x	1	1	0	0	0	0	Cursor Coefficient 49 Psuedo Port 2
	x	x	1	1	0	0	0	1	Cursor Coefficient 50 Psuedo Port 2
	x	x	1	1	0	0	1	0	Cursor Coefficient 51 Psuedo Port 2
	x	x	1	1	0	0	1	1	Cursor Coefficient 52 Psuedo Port 2
	x	x	1	1	0	1	0	0	Cursor Coefficient 53 Psuedo Port 2
	x	x	1	1	0	1	0	1	Cursor Coefficient 54 Psuedo Port 2
	x	x	1	1	0	1	1	0	Cursor Coefficient 55 Psuedo Port 2
	x	x	1	1	0	1	1	1	Cursor Coefficient 56 Psuedo Port 2
	x	x	1	1	1	0	0	0	Cursor Coefficient 57 Psuedo Port 2
	x	x	1	1	1	0	0	1	Cursor Coefficient 58 Psuedo Port 2
	x	x	1	1	1	0	1	0	Cursor Coefficient 59 Psuedo Port 2
	x	x	1	1	1	0	1	1	Cursor Coefficient 60 Psuedo Port 2
	x	x	1	1	1	1	0	0	Cursor Coefficient 61 Psuedo Port 2
	x	x	1	1	1	1	0	1	Cursor Coefficient 62 Psuedo Port 2
	x	x	1	1	1	1	1	0	Cursor Coefficient 63 Psuedo Port 2
	x	x	1	1	1	1	1	1	Cursor Coefficient 64 Psuedo Port 2

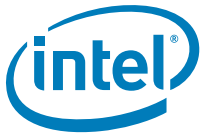


Table 6-2 Register Bit Level Details (Sheet 13 of 17)

Physical Pseudo Port 2 Parameter Register 5	x	x	0	0	0	0	0	0	Pre-Cursor Coefficient 1 Psuedo Port 2
	x	x	0	0	0	0	0	1	Pre-Cursor Coefficient 2 Psuedo Port 2
	x	x	0	0	0	0	1	0	Pre-Cursor Coefficient 3 Psuedo Port 2
	x	x	0	0	0	0	1	1	Pre-Cursor Coefficient 4 Psuedo Port 2
	x	x	0	0	0	1	0	0	Pre-Cursor Coefficient 5 Psuedo Port 2
	x	x	0	0	0	1	0	1	Pre-Cursor Coefficient 6 Psuedo Port 2
	x	x	0	0	0	1	1	0	Pre-Cursor Coefficient 7 Psuedo Port 2
	x	x	0	0	0	1	1	1	Pre-Cursor Coefficient 8 Psuedo Port 2
	x	x	0	0	1	0	0	0	Pre-Cursor Coefficient 9 Psuedo Port 2
	x	x	0	0	1	0	0	1	Pre-Cursor Coefficient 10 Psuedo Port 2
	x	x	0	0	1	0	1	0	Pre-Cursor Coefficient 11 Psuedo Port 2
	x	x	0	0	1	0	1	1	Pre-Cursor Coefficient 12 Psuedo Port 2
	x	x	0	0	1	1	0	0	Pre-Cursor Coefficient 13 Psuedo Port 2
	x	x	0	0	1	1	0	1	Pre-Cursor Coefficient 14 Psuedo Port 2
	x	x	0	0	1	1	1	0	Pre-Cursor Coefficient 15 Psuedo Port 2
	x	x	0	0	1	1	1	1	Pre-Cursor Coefficient 16 Psuedo Port 2
	x	x	0	1	0	0	0	0	Pre-Cursor Coefficient 17 Psuedo Port 2
	x	x	0	1	0	0	0	1	Pre-Cursor Coefficient 18 Psuedo Port 2
	x	x	0	1	0	0	1	0	Pre-Cursor Coefficient 19 Psuedo Port 2
	x	x	0	1	0	0	1	1	Pre-Cursor Coefficient 20 Psuedo Port 2
	x	x	0	1	0	1	0	0	Pre-Cursor Coefficient 21 Psuedo Port 2
	x	x	0	1	0	1	0	1	Pre-Cursor Coefficient 22 Psuedo Port 2
	x	x	0	1	0	1	1	0	Pre-Cursor Coefficient 23 Psuedo Port 2
	x	x	0	1	0	1	1	1	Pre-Cursor Coefficient 24 Psuedo Port 2
	x	x	0	1	1	0	0	0	Pre-Cursor Coefficient 25 Psuedo Port 2
	x	x	0	1	1	0	0	1	Pre-Cursor Coefficient 26 Psuedo Port 2
	x	x	0	1	1	0	1	0	Pre-Cursor Coefficient 27 Psuedo Port 2
	x	x	0	1	1	0	1	1	Pre-Cursor Coefficient 28 Psuedo Port 2
	x	x	0	1	1	1	0	0	Pre-Cursor Coefficient 29 Psuedo Port 2
	x	x	0	1	1	1	0	1	Pre-Cursor Coefficient 30 Psuedo Port 2
	x	x	0	1	1	1	1	0	Pre-Cursor Coefficient 31 Psuedo Port 2
	x	x	0	1	1	1	1	1	Pre-Cursor Coefficient 32 Psuedo Port 2
	x	x	1	0	0	0	0	0	Pre-Cursor Coefficient 33 Psuedo Port 2
	x	x	1	0	0	0	0	1	Pre-Cursor Coefficient 34 Psuedo Port 2
	x	x	1	0	0	0	1	0	Pre-Cursor Coefficient 35 Psuedo Port 2
	x	x	1	0	0	0	1	1	Pre-Cursor Coefficient 36 Psuedo Port 2
	x	x	1	0	0	1	0	0	Pre-Cursor Coefficient 37 Psuedo Port 2
	x	x	1	0	0	1	0	1	Pre-Cursor Coefficient 38 Psuedo Port 2
	x	x	1	0	0	1	1	0	Pre-Cursor Coefficient 39 Psuedo Port 2
	x	x	1	0	0	1	1	1	Pre-Cursor Coefficient 40 Psuedo Port 2
	x	x	1	0	1	0	0	0	Pre-Cursor Coefficient 41 Psuedo Port 2
	x	x	1	0	1	0	0	1	Pre-Cursor Coefficient 42 Psuedo Port 2
	x	x	1	0	1	0	1	0	Pre-Cursor Coefficient 43 Psuedo Port 2
	x	x	1	0	1	0	1	1	Pre-Cursor Coefficient 44 Psuedo Port 2
	x	x	1	0	1	1	0	0	Pre-Cursor Coefficient 45 Psuedo Port 2
	x	x	1	0	1	1	0	1	Pre-Cursor Coefficient 46 Psuedo Port 2
	x	x	1	0	1	1	1	0	Pre-Cursor Coefficient 47 Psuedo Port 2
	x	x	1	0	1	1	1	1	Pre-Cursor Coefficient 48 Psuedo Port 2
	x	x	1	1	0	0	0	0	Pre-Cursor Coefficient 49 Psuedo Port 2
	x	x	1	1	0	0	0	1	Pre-Cursor Coefficient 50 Psuedo Port 2
	x	x	1	1	0	0	1	0	Pre-Cursor Coefficient 51 Psuedo Port 2
	x	x	1	1	0	0	1	1	Pre-Cursor Coefficient 52 Psuedo Port 2
	x	x	1	1	0	1	0	0	Pre-Cursor Coefficient 53 Psuedo Port 2
	x	x	1	1	0	1	0	1	Pre-Cursor Coefficient 54 Psuedo Port 2
	x	x	1	1	0	1	1	0	Pre-Cursor Coefficient 55 Psuedo Port 2
	x	x	1	1	0	1	1	1	Pre-Cursor Coefficient 56 Psuedo Port 2
	x	x	1	1	1	0	0	0	Pre-Cursor Coefficient 57 Psuedo Port 2
	x	x	1	1	1	0	0	1	Pre-Cursor Coefficient 58 Psuedo Port 2
	x	x	1	1	1	0	1	0	Pre-Cursor Coefficient 59 Psuedo Port 2
	x	x	1	1	1	0	1	1	Pre-Cursor Coefficient 60 Psuedo Port 2
	x	x	1	1	1	1	0	0	Pre-Cursor Coefficient 61 Psuedo Port 2
	x	x	1	1	1	1	0	1	Pre-Cursor Coefficient 62 Psuedo Port 2
	x	x	1	1	1	1	1	0	Pre-Cursor Coefficient 63 Psuedo Port 2
	x	x	1	1	1	1	1	1	Pre-Cursor Coefficient 64 Psuedo Port 2

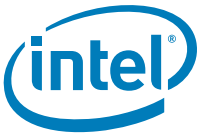


Table 6-2 Register Bit Level Details (Sheet 14 of 17)

Physical Pseudo Port 2 Parameter Register 6	x	x	0	0	0	0	0	0	Post-Cursor Coefficient 1 Psuedo Port 2
	x	x	0	0	0	0	0	1	Post-Cursor Coefficient 2 Psuedo Port 2
	x	x	0	0	0	0	1	0	Post-Cursor Coefficient 3 Psuedo Port 2
	x	x	0	0	0	0	1	1	Post-Cursor Coefficient 4 Psuedo Port 2
	x	x	0	0	0	1	0	0	Post-Cursor Coefficient 5 Psuedo Port 2
	x	x	0	0	0	1	0	1	Post-Cursor Coefficient 6 Psuedo Port 2
	x	x	0	0	0	1	1	0	Post-Cursor Coefficient 7 Psuedo Port 2
	x	x	0	0	0	1	1	1	Post-Cursor Coefficient 8 Psuedo Port 2
	x	x	0	0	1	0	0	0	Post-Cursor Coefficient 9 Psuedo Port 2
	x	x	0	0	1	0	0	1	Post-Cursor Coefficient 10 Psuedo Port 2
	x	x	0	0	1	0	1	0	Post-Cursor Coefficient 11 Psuedo Port 2
	x	x	0	0	1	0	1	1	Post-Cursor Coefficient 12 Psuedo Port 2
	x	x	0	0	1	1	0	0	Post-Cursor Coefficient 13 Psuedo Port 2
	x	x	0	0	1	1	0	1	Post-Cursor Coefficient 14 Psuedo Port 2
	x	x	0	0	1	1	1	0	Post-Cursor Coefficient 15 Psuedo Port 2
	x	x	0	0	1	1	1	1	Post-Cursor Coefficient 16 Psuedo Port 2
	x	x	0	1	0	0	0	0	Post-Cursor Coefficient 17 Psuedo Port 2
	x	x	0	1	0	0	0	1	Post-Cursor Coefficient 18 Psuedo Port 2
	x	x	0	1	0	0	1	0	Post-Cursor Coefficient 19 Psuedo Port 2
	x	x	0	1	0	0	1	1	Post-Cursor Coefficient 20 Psuedo Port 2
	x	x	0	1	0	1	0	0	Post-Cursor Coefficient 21 Psuedo Port 2
	x	x	0	1	0	1	0	1	Post-Cursor Coefficient 22 Psuedo Port 2
	x	x	0	1	0	1	1	0	Post-Cursor Coefficient 23 Psuedo Port 2
	x	x	0	1	0	1	1	1	Post-Cursor Coefficient 24 Psuedo Port 2
	x	x	0	1	1	0	0	0	Post-Cursor Coefficient 25 Psuedo Port 2
	x	x	0	1	1	0	0	1	Post-Cursor Coefficient 26 Psuedo Port 2
	x	x	0	1	1	0	1	0	Post-Cursor Coefficient 27 Psuedo Port 2
	x	x	0	1	1	0	1	1	Post-Cursor Coefficient 28 Psuedo Port 2
	x	x	0	1	1	1	0	0	Post-Cursor Coefficient 29 Psuedo Port 2
	x	x	0	1	1	1	0	1	Post-Cursor Coefficient 30 Psuedo Port 2
	x	x	0	1	1	1	1	0	Post-Cursor Coefficient 31 Psuedo Port 2
	x	x	0	1	1	1	1	1	Post-Cursor Coefficient 32 Psuedo Port 2
	x	x	1	0	0	0	0	0	Post-Cursor Coefficient 33 Psuedo Port 2
	x	x	1	0	0	0	0	1	Post-Cursor Coefficient 34 Psuedo Port 2
	x	x	1	0	0	0	1	0	Post-Cursor Coefficient 35 Psuedo Port 2
	x	x	1	0	0	0	1	1	Post-Cursor Coefficient 36 Psuedo Port 2
	x	x	1	0	0	1	0	0	Post-Cursor Coefficient 37 Psuedo Port 2
	x	x	1	0	0	1	0	1	Post-Cursor Coefficient 38 Psuedo Port 2
	x	x	1	0	0	1	1	0	Post-Cursor Coefficient 39 Psuedo Port 2
	x	x	1	0	0	1	1	1	Post-Cursor Coefficient 40 Psuedo Port 2
	x	x	1	0	1	0	0	0	Post-Cursor Coefficient 41 Psuedo Port 2
	x	x	1	0	1	0	0	1	Post-Cursor Coefficient 42 Psuedo Port 2
	x	x	1	0	1	0	1	0	Post-Cursor Coefficient 43 Psuedo Port 2
	x	x	1	0	1	0	1	1	Post-Cursor Coefficient 44 Psuedo Port 2
	x	x	1	0	1	1	0	0	Post-Cursor Coefficient 45 Psuedo Port 2
	x	x	1	0	1	1	0	1	Post-Cursor Coefficient 46 Psuedo Port 2
	x	x	1	0	1	1	1	0	Post-Cursor Coefficient 47 Psuedo Port 2
	x	x	1	0	1	1	1	1	Post-Cursor Coefficient 48 Psuedo Port 2
	x	x	1	1	0	0	0	0	Post-Cursor Coefficient 49 Psuedo Port 2
	x	x	1	1	0	0	0	1	Post-Cursor Coefficient 50 Psuedo Port 2
	x	x	1	1	0	0	1	0	Post-Cursor Coefficient 51 Psuedo Port 2
	x	x	1	1	0	0	1	1	Post-Cursor Coefficient 52 Psuedo Port 2
	x	x	1	1	0	1	0	0	Post-Cursor Coefficient 53 Psuedo Port 2
	x	x	1	1	0	1	0	1	Post-Cursor Coefficient 54 Psuedo Port 2
	x	x	1	1	0	1	1	0	Post-Cursor Coefficient 55 Psuedo Port 2
	x	x	1	1	0	1	1	1	Post-Cursor Coefficient 56 Psuedo Port 2
	x	x	1	1	1	0	0	0	Post-Cursor Coefficient 57 Psuedo Port 2
	x	x	1	1	1	0	0	1	Post-Cursor Coefficient 58 Psuedo Port 2
	x	x	1	1	1	0	1	0	Post-Cursor Coefficient 59 Psuedo Port 2
	x	x	1	1	1	0	1	1	Post-Cursor Coefficient 60 Psuedo Port 2
	x	x	1	1	1	1	0	0	Post-Cursor Coefficient 61 Psuedo Port 2
	x	x	1	1	1	1	0	1	Post-Cursor Coefficient 62 Psuedo Port 2
	x	x	1	1	1	1	1	0	Post-Cursor Coefficient 63 Psuedo Port 2
	x	x	1	1	1	1	1	1	Post-Cursor Coefficient 64 Psuedo Port 2

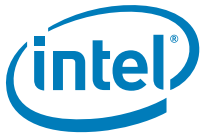


Table 6-2 Register Bit Level Details (Sheet 15 of 17)

Physical Pseudo Port 2 Parameter Register 7	x	x	0	0	0	0	0	0	Cursor Coefficient 1 Psuedo Port 1
	x	x	0	0	0	0	0	1	Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Cursor Coefficient 64 Psuedo Port 1

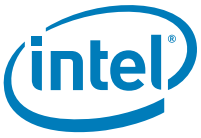


Table 6-2 Register Bit Level Details (Sheet 16 of 17)

Physical Pseudo Port 2 Parameter Register 8	x	x	0	0	0	0	0	0	Pre-Cursor Coefficient 1 Psuedo Port 1
	x	x	0	0	0	0	0	1	Pre-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Pre-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Pre-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Pre-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Pre-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Pre-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Pre-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Pre-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Pre-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Pre-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Pre-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Pre-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Pre-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Pre-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Pre-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Pre-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Pre-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Pre-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Pre-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Pre-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Pre-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Pre-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Pre-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Pre-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Pre-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Pre-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Pre-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Pre-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Pre-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Pre-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Pre-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Pre-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Pre-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Pre-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Pre-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Pre-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Pre-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Pre-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Pre-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Pre-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Pre-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Pre-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Pre-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Pre-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Pre-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Pre-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Pre-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Pre-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Pre-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Pre-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Pre-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Pre-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Pre-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Pre-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Pre-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Pre-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Pre-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Pre-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Pre-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Pre-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Pre-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Pre-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Pre-Cursor Coefficient 64 Psuedo Port 1

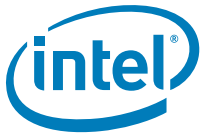


Table 6-2 Register Bit Level Details (Sheet 17 of 17)

Physical Pseudo Port 2 Parameter Register 9	x	x	0	0	0	0	0	0	Post-Cursor Coefficient 1 Psuedo Port 1
	x	x	0	0	0	0	0	1	Post-Cursor Coefficient 2 Psuedo Port 1
	x	x	0	0	0	0	1	0	Post-Cursor Coefficient 3 Psuedo Port 1
	x	x	0	0	0	0	1	1	Post-Cursor Coefficient 4 Psuedo Port 1
	x	x	0	0	0	1	0	0	Post-Cursor Coefficient 5 Psuedo Port 1
	x	x	0	0	0	1	0	1	Post-Cursor Coefficient 6 Psuedo Port 1
	x	x	0	0	0	1	1	0	Post-Cursor Coefficient 7 Psuedo Port 1
	x	x	0	0	0	1	1	1	Post-Cursor Coefficient 8 Psuedo Port 1
	x	x	0	0	1	0	0	0	Post-Cursor Coefficient 9 Psuedo Port 1
	x	x	0	0	1	0	0	1	Post-Cursor Coefficient 10 Psuedo Port 1
	x	x	0	0	1	0	1	0	Post-Cursor Coefficient 11 Psuedo Port 1
	x	x	0	0	1	0	1	1	Post-Cursor Coefficient 12 Psuedo Port 1
	x	x	0	0	1	1	0	0	Post-Cursor Coefficient 13 Psuedo Port 1
	x	x	0	0	1	1	0	1	Post-Cursor Coefficient 14 Psuedo Port 1
	x	x	0	0	1	1	1	0	Post-Cursor Coefficient 15 Psuedo Port 1
	x	x	0	0	1	1	1	1	Post-Cursor Coefficient 16 Psuedo Port 1
	x	x	0	1	0	0	0	0	Post-Cursor Coefficient 17 Psuedo Port 1
	x	x	0	1	0	0	0	1	Post-Cursor Coefficient 18 Psuedo Port 1
	x	x	0	1	0	0	1	0	Post-Cursor Coefficient 19 Psuedo Port 1
	x	x	0	1	0	0	1	1	Post-Cursor Coefficient 20 Psuedo Port 1
	x	x	0	1	0	1	0	0	Post-Cursor Coefficient 21 Psuedo Port 1
	x	x	0	1	0	1	0	1	Post-Cursor Coefficient 22 Psuedo Port 1
	x	x	0	1	0	1	1	0	Post-Cursor Coefficient 23 Psuedo Port 1
	x	x	0	1	0	1	1	1	Post-Cursor Coefficient 24 Psuedo Port 1
	x	x	0	1	1	0	0	0	Post-Cursor Coefficient 25 Psuedo Port 1
	x	x	0	1	1	0	0	1	Post-Cursor Coefficient 26 Psuedo Port 1
	x	x	0	1	1	0	1	0	Post-Cursor Coefficient 27 Psuedo Port 1
	x	x	0	1	1	0	1	1	Post-Cursor Coefficient 28 Psuedo Port 1
	x	x	0	1	1	1	0	0	Post-Cursor Coefficient 29 Psuedo Port 1
	x	x	0	1	1	1	0	1	Post-Cursor Coefficient 30 Psuedo Port 1
	x	x	0	1	1	1	1	0	Post-Cursor Coefficient 31 Psuedo Port 1
	x	x	0	1	1	1	1	1	Post-Cursor Coefficient 32 Psuedo Port 1
	x	x	1	0	0	0	0	0	Post-Cursor Coefficient 33 Psuedo Port 1
	x	x	1	0	0	0	0	1	Post-Cursor Coefficient 34 Psuedo Port 1
	x	x	1	0	0	0	1	0	Post-Cursor Coefficient 35 Psuedo Port 1
	x	x	1	0	0	0	1	1	Post-Cursor Coefficient 36 Psuedo Port 1
	x	x	1	0	0	1	0	0	Post-Cursor Coefficient 37 Psuedo Port 1
	x	x	1	0	0	1	0	1	Post-Cursor Coefficient 38 Psuedo Port 1
	x	x	1	0	0	1	1	0	Post-Cursor Coefficient 39 Psuedo Port 1
	x	x	1	0	0	1	1	1	Post-Cursor Coefficient 40 Psuedo Port 1
	x	x	1	0	1	0	0	0	Post-Cursor Coefficient 41 Psuedo Port 1
	x	x	1	0	1	0	0	1	Post-Cursor Coefficient 42 Psuedo Port 1
	x	x	1	0	1	0	1	0	Post-Cursor Coefficient 43 Psuedo Port 1
	x	x	1	0	1	0	1	1	Post-Cursor Coefficient 44 Psuedo Port 1
	x	x	1	0	1	1	0	0	Post-Cursor Coefficient 45 Psuedo Port 1
	x	x	1	0	1	1	0	1	Post-Cursor Coefficient 46 Psuedo Port 1
	x	x	1	0	1	1	1	0	Post-Cursor Coefficient 47 Psuedo Port 1
	x	x	1	0	1	1	1	1	Post-Cursor Coefficient 48 Psuedo Port 1
	x	x	1	1	0	0	0	0	Post-Cursor Coefficient 49 Psuedo Port 1
	x	x	1	1	0	0	0	1	Post-Cursor Coefficient 50 Psuedo Port 1
	x	x	1	1	0	0	1	0	Post-Cursor Coefficient 51 Psuedo Port 1
	x	x	1	1	0	0	1	1	Post-Cursor Coefficient 52 Psuedo Port 1
	x	x	1	1	0	1	0	0	Post-Cursor Coefficient 53 Psuedo Port 1
	x	x	1	1	0	1	0	1	Post-Cursor Coefficient 54 Psuedo Port 1
	x	x	1	1	0	1	1	0	Post-Cursor Coefficient 55 Psuedo Port 1
	x	x	1	1	0	1	1	1	Post-Cursor Coefficient 56 Psuedo Port 1
	x	x	1	1	1	0	0	0	Post-Cursor Coefficient 57 Psuedo Port 1
	x	x	1	1	1	0	0	1	Post-Cursor Coefficient 58 Psuedo Port 1
	x	x	1	1	1	0	1	0	Post-Cursor Coefficient 59 Psuedo Port 1
	x	x	1	1	1	0	1	1	Post-Cursor Coefficient 60 Psuedo Port 1
	x	x	1	1	1	1	0	0	Post-Cursor Coefficient 61 Psuedo Port 1
	x	x	1	1	1	1	0	1	Post-Cursor Coefficient 62 Psuedo Port 1
	x	x	1	1	1	1	1	0	Post-Cursor Coefficient 63 Psuedo Port 1
	x	x	1	1	1	1	1	1	Post-Cursor Coefficient 64 Psuedo Port 1

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